AN1299
Application note

L638xE tricks and tips

Introduction

The ST L638xE family includes five control ICs: L6384E, L6385E, L6386E, L6387E and L6388E.

They are designed in BCD offline technology and are able to operate at voltage up to 600 V. The logic inputs are CMOS logic compatible and the driving stages can source up to 400 mA and sink 650 mA.

The bootstrap diode is integrated inside the ICs which helps to reduce the number of PCB parts and to increase the layout flexibility.

Topics covered:

- Device family
- Internal diode structure
- How to select C_{boot}
- Parasitic elements in the half-bridge topology
- How to manage below-ground voltage on the OUT pin:
  - OUT pin voltage that persists below the signal ground
  - Undershoot spike on the OUT pin
  - Tricks and layout suggestions
- L6386E: how to deal with signal ground and power ground

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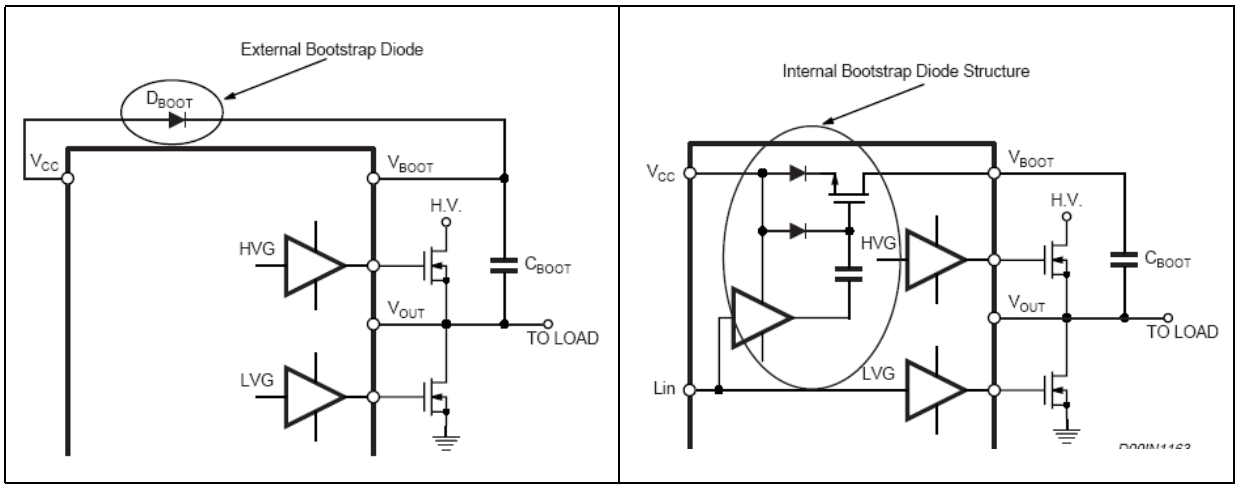
1 Internal diode structure

Figure 1. External bootstrap diode schematic **Figure 2. Internal bootstrap diode schematic**



A floating supply is required to drive the high-voltage section and the high-side switch gate. For this reason we must use the bootstrap principle, normally accomplished by a high-voltage fast-recovery diode (*Figure 1*). The bootstrap capacitor is charged when the Vout goes below the IC supply voltage. In this situation the current flows from the IC supply (Vcc pin) to the capacitor (*Figure 3*). When the OUT pin is pulled up near to the high-voltage rail (the low-side switch is turned off and the high-side is switched on), the diode is reverse biased and the capacitor can "fly up" to the level of the high-voltage bus plus Vcc. The high-voltage section is supplied only by the bootstrap capacitor.

In the L638xE family a patented integrated structure replaces the external diode. It is composed of a high-voltage DMOS (typical $R_{DS(on)}$ 125 Ω) driven synchronously with the low-side driver (LVG), with a diode in series, as indicated in *Figure 2*.

When the internal bootstrap structure is used we have to remember that:

1. The "internal diode" is a structure and not an integrated discrete diode which means that the diode structure is turned on (and it behaves like an external diode) only when the low-side driver is on.
2. When the low-side driver is turned on, the OUT pin voltage must be below the IC supply, otherwise the current cannot flow from the supply to the bootstrap capacitor (*Figure 3*).

Figure 3. Bootstrap capacitor charging path

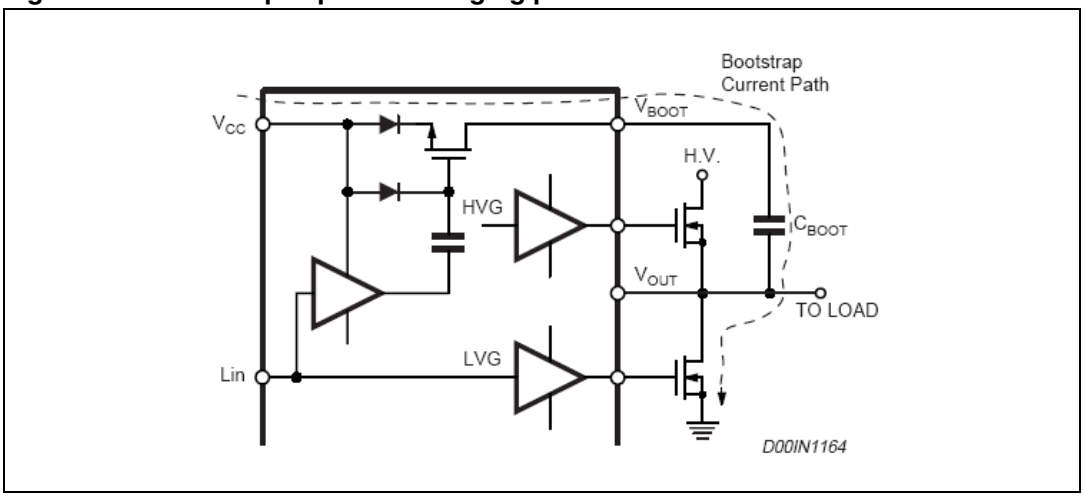


Figure 4 shows an example in which the internal bootstrap diode cannot be used. When the low-side driver is on (*Figure 5*), the voltage at the OUT pin is held to the high-voltage bus and the current cannot charge the bootstrap capacitor. The OUT pin voltage goes close to 0 V only when Vinput is low (Vout=-V_f - R_{sense}*I_{load}), but in this situation the internal diode is off and the charging current cannot flow in the capacitor.

For more detailed information on the internal diode behavior see AN1263 "Using the internal bootstrap charge capability of the L638xE in driving a six transistor inverter bridge".

Figure 4. Example of a mandatory external diode

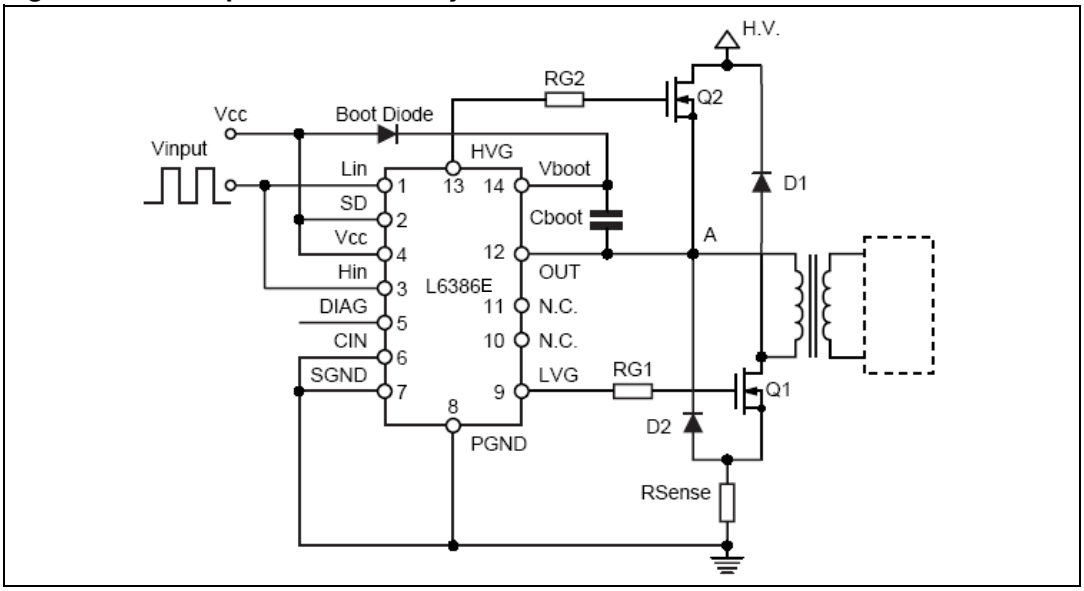


Figure 5. Example of a mandatory external diode - Vinput HIGH

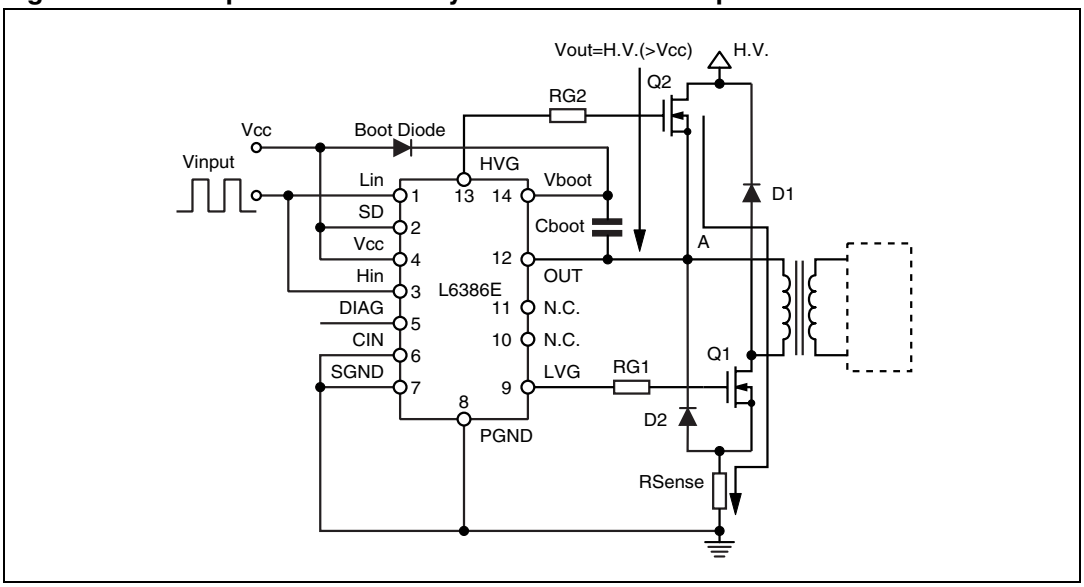
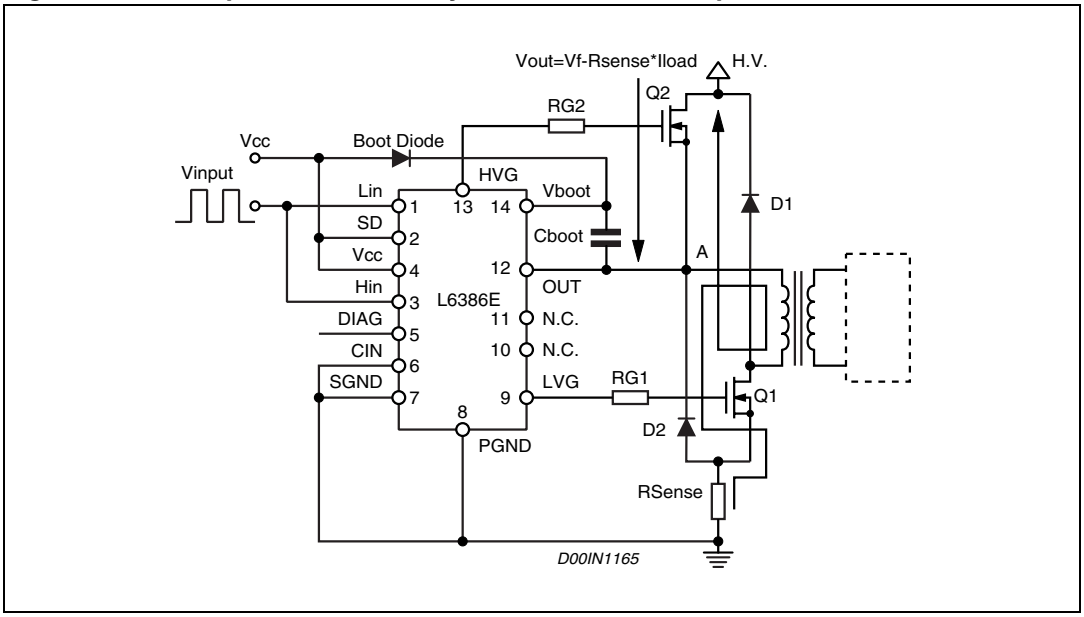


Figure 6. Example of a mandatory external diode - Vinput LOW



2 How to select C_{boot}

As previously discussed, when the internal bootstrap diode is used, the bootstrap capacitor is charged every time the low-side driver is on and the OUT pin goes below the IC supply voltage.

The capacitor is discharged only when the high-side switch is turned on. This capacitor works as power supply for the high-voltage section.

Let us discuss how to select the right capacitor value. The dimensioning procedure we are going to describe is valid for both cases, with or without the external diode.

The first parameter to take into account is the maximum voltage drop that we have to guarantee when the high-side switch is in an on state.

The maximum allowable voltage drop (ΔV_{boot}) depends on the minimum gate drive voltage (for the high-side switch) that we want to maintain. If V_{gs_min} is the minimum gate source voltage, the capacitor drop must be:

Equation 1

$$\Delta V_{boot} = V_{CC} - V_F - V_{gs\_min}$$

V_{cc} : IC voltage supply

V_F : bootstrap diode forward voltage

The capacitor size is calculated by the formula:

Equation 2

$$C_{boot} = \frac{Q_{tot}}{\Delta V_{boot}}$$

Q_{tot} : total amount of the charge supplied by the capacitor. This is evaluated taking into account the following factors:

1. Q_{gate}: high-side switch total gate charge
2. I_{lk_gs}: high-side switch gate-source leakage current
3. I_{lk_cap}: bootstrap capacitor leakage current
4. I_{qbs}: bootstrapped section quiescent current
5. I_{lk}: bootstrapped section leakage current
6. Q_{ls}: charge required by the internal level shifter (3 nC for all L638xE drivers)
7. T_{on}: high-side switch on time
8. I_{lk_diode}: External diode leakage current (if it is used)

The total charge supplied by the bootstrap capacitor is:

Equation 3

$$Q_{tot} = Q_{gate} + (I_{lk\_cap} + I_{lk\_gs} + I_{qbs} + I_{lk} + I_{lk\_diode}) \cdot T_{on} + Q_{ls}$$

The capacitor leakage current is important only if an electrolytic capacitor is used, otherwise this term can be neglected (e.g. with a ceramic capacitor).

When the internal diode is used, the DMOS $R_{DS(on)}$ introduces an additional voltage drop that can be low at low switching frequency. Increasing the frequency, this drop can be evaluated as follows:

Equation 4

$$V_{drop} = I_{charge} \cdot R_{DS(on)} = \frac{Q_{tot}}{T_{charge}} \cdot R_{DS(on)}$$

I_{charge}: capacitor charging current

$R_{DS(on)}$: DMOS drain-source typical on resistance

T_{charge}: capacitor charging time (it is the low-side turn-on time).

This drop must be taken into account when the maximum ΔV_{boot} is calculated. If this drop is too high or the circuit topology does not allow a sufficient charging time, an external fast recovery diode can be used.

Example:

Let's evaluate the bootstrap capacitor size when the internal diode is used.

Data:

- Q_{gate} = 70 nC (STGW12NB60H)
- I_{lk_gs} = 100 nA
- I_{qbs} = 200 µA (datasheet L6386E)
- I_{lk} = 10 µA (datasheet L6386E)
- Q_{ls} = 3 nC
- T_{on} = 100 µs

Capacitor leakage current is not considered because we assume that a ceramic capacitor is used and not an electrolytic one.

If the maximum allowable voltage drop on the bootstrap capacitor is 1 V during the high-side switch-on state, the minimum capacitor size is:

Equation 5

$$C_{boot} = \frac{Q_{tot}}{\Delta V_{boot}} = \frac{94nC}{1\ V} = 94nF$$

The voltage drop due to the internal DMOS $R_{DS(on)}$ is nearly:

Equation 6

$$V_{drop} = \frac{Q_{tot}}{T_{charge}} \cdot R_{DS(on)} = \frac{94nC}{100\mu s} \cdot 125\Omega = 117mV$$

and can be neglected. We have assumed the capacitor charging time equal to the high side on time (duty cycle 50%).

According to different bootstrap capacitor sizes we may have the following drops:

- $100nF \rightarrow \Delta V_{boot} = \frac{Q_{tot}}{C_{boot}} = 0.93V$
- $150nF \rightarrow \Delta V_{boot} = \frac{Q_{tot}}{C_{boot}} = 0.62V$

- $220nF \rightarrow \Delta V_{boot} = \frac{Q_{tot}}{C_{boot}} = 0.42V$

Suggested values are within the range of 100 nF - 570 nF but the right value must be selected according to the application in which the device is used. When the capacitor size is too big, the bootstrap charging time is slowed and the low-side on time (i.e. the "internal diode" on time) might be not long enough to reach the right bootstrap voltage.

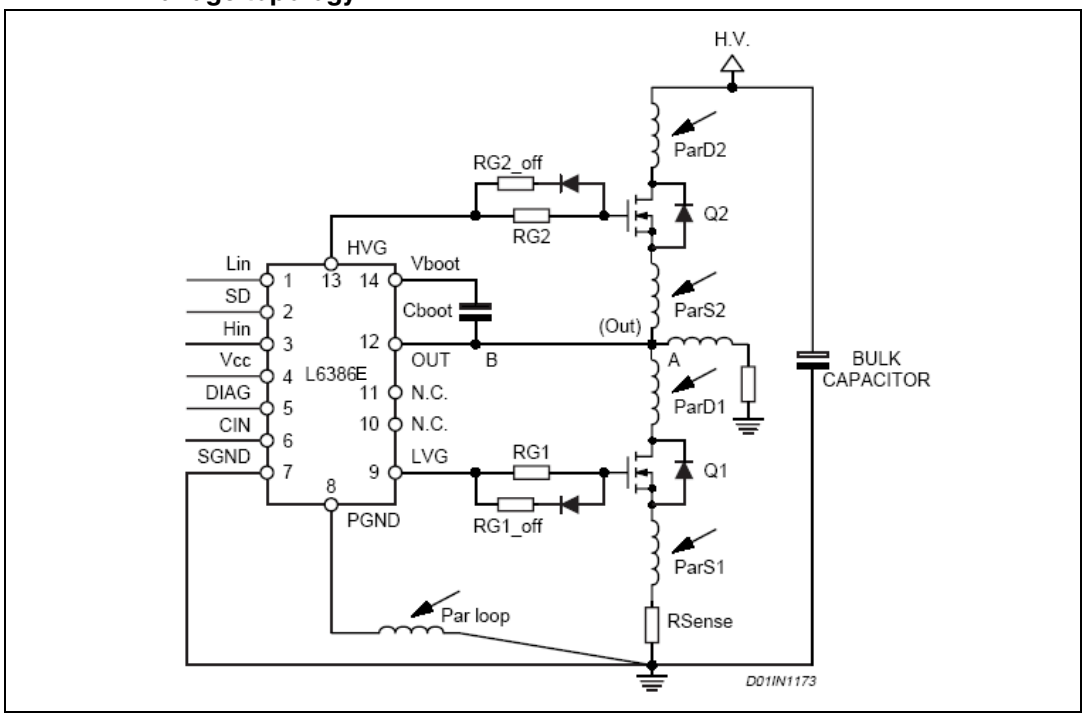
3 Parasitic elements in the half-bridge topology

Parasitic elements exist inside a half-bridge driver circuit and they have to be considered because rapid changes of switching currents induce voltage transients across all the parasitic components.

In the following paragraphs we are going to describe the use of L6386E in a typical half-bridge application and the layout parasitic elements to be minimized in order to improve the application behavior (see *Figure 7*).

We have taken the L6386E device as example, but our considerations can also be used for all L638xE drivers.

Figure 7. Main parasitic elements that must be taken into account inside the half-bridge topology



4 To manage below-ground voltage on the OUT pin

We have to take care of the below-ground voltage on the OUT pin because they are really pernicious. There are two main issues (*Figure 9*):

1. OUT pin voltage persists below the signal ground reference during the entire time in which the low-side freewheeling diode is in conduction state (static condition)
2. Undershoot spike on the OUT pin that appears during the commutation pattern (dynamic condition)

In the following sections let's analyze both the issues and what could happen to the IC.

4.1 OUT pin voltage that persists below the signal ground

Figure 8. Static below-ground voltage example

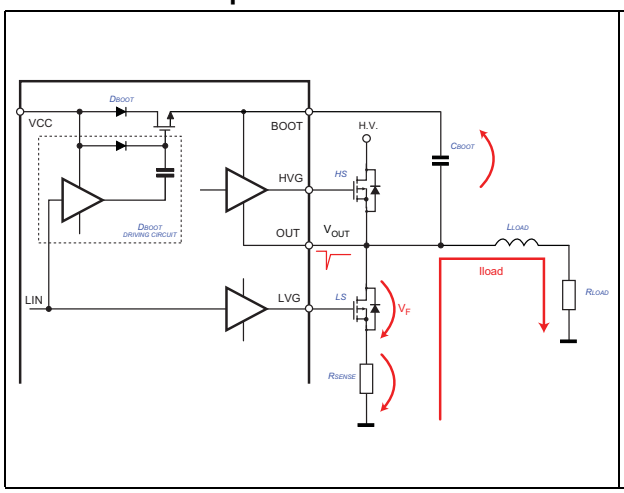
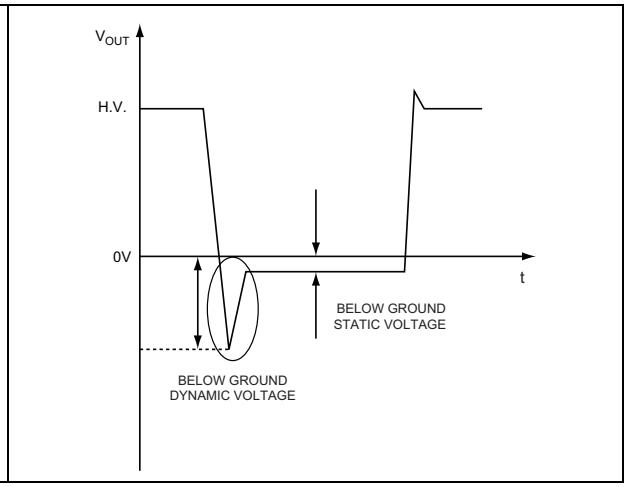


Figure 9. Below-ground voltage on OUT pin



In static mode the OUT pin can sustain below-ground voltages down to -3 V (absolute maximum rating). Within this limit, a negative voltage on the OUT pin can cause the bootstrap capacitor to overcharge. This condition happens when the load current flows in the direction shown in *Figure 8*. The high side is off and the low-side freewheeling diode is on.

In this condition the voltage between the OUT pin and the ground is:

Equation 7

$$V_{out} = -(R_{sense} + R_{trace}) \cdot I_{load} - V_f$$

Where V_f is the freewheeling diode forward voltage, R_{trace} is the parasitic trace resistance, R_{sense} the sense resistor and I_{load} is the load current. We have not mentioned the parasitic trace inductance because we are not dealing with dynamic undershoot voltage.

The voltage across the C_{boot} is:

Equation 8

$$V_{boot} = V_{CC} - V_{out} = V_{CC} + (R_{sense} + R_{trace}) \cdot I_{load} + V_f$$

V_{boot} must be less than 17 V (recommended operating condition for all L638xE drivers). The bootstrap capacitor acts as the power supply for the internal high voltage driver, and if this voltage goes above the recommended condition, the device may not work properly.

In order to avoid this undesired phenomenon we suggest the following guidelines:

- Maintain a "safety margin" when the V_{cc} is selected. For example, if we use V_{cc} = 15 V and we want to avoid that the bootstrap capacitor becomes overcharged (i.e. charged over 17 V), the OUT pin should not go below ground more than - 2 V. The higher the V_{cc}, the lower the below-ground voltage on the OUT pin.
- Select R_{sense} and minimize R_{trace} in order to satisfy the the following relation:

Equation 9

$$V_{boot} = V_{CC} - V_{out} = V_{CC} + (R_{sense} + R_{trace}) \cdot I_{load} + V_f < 17V$$

4.2 Undershoot spike on the OUT pin

If the OUT pin undershoot spike has a time length that is in the order of tenths of nanoseconds the bootstrap capacitor cannot become overcharged.

Figure 10. Equivalent internal bootstrap charging circuit

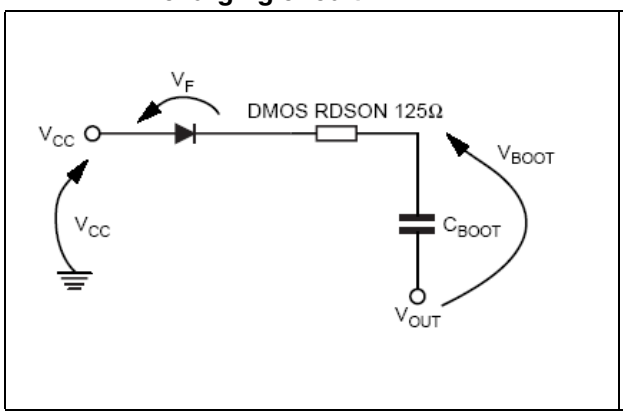
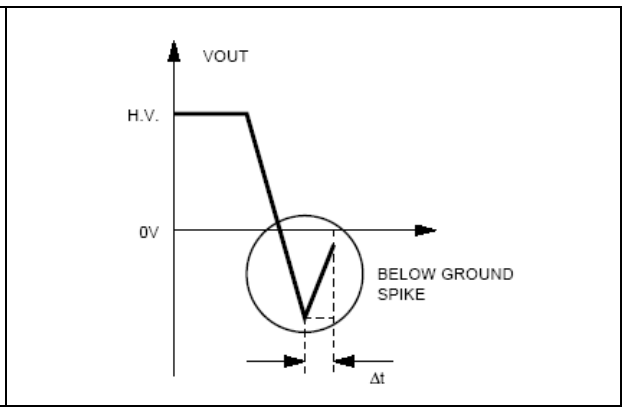


Figure 11. Dynamic below-ground voltage



We can evaluate the maximum below-ground duration that can lead to capacitor overcharge. Let us assume that the below-ground spike does not have a triangular shape but a square shape, like the dotted line in the *Figure 11* (worst case). If we have:

- V_{cc} = 15 V
- C_{boot} = 100 nF
- V_f = 0.7 V
- V_{out} = 18 V (below-ground spike on the OUT pin)
- ΔV_{boot} =17 V - 15 V = 2 V (maximum allowable capacitor overcharge voltage)

The maximum below-ground spike duration is:

Equation 10

$$\Delta t = R_{DS(on)} \cdot C_{boot} \cdot Ln\left(\frac{V_{out} - V_f}{V_{out} - V_f - \Delta V_{boot}}\right) \cong 1.5\mu s$$

It is much more than some tenths of nanoseconds. Note that in this example we use the internal bootstrap diode.

The example above demonstrates that short undershoot spikes on the OUT pin do not lead to bootstrap overcharge.

Note that if an external diode is adopted and no resistors in series with the diode are used, the Δt will be shorter and the bootstrap overcharging could be significant.

The undershoot spike is caused by the parasitic inductance in the tracks between the OUT node and ground, we have called them ParD1 and ParS1 in *Figure 7*.

Now we will analyze the following points:

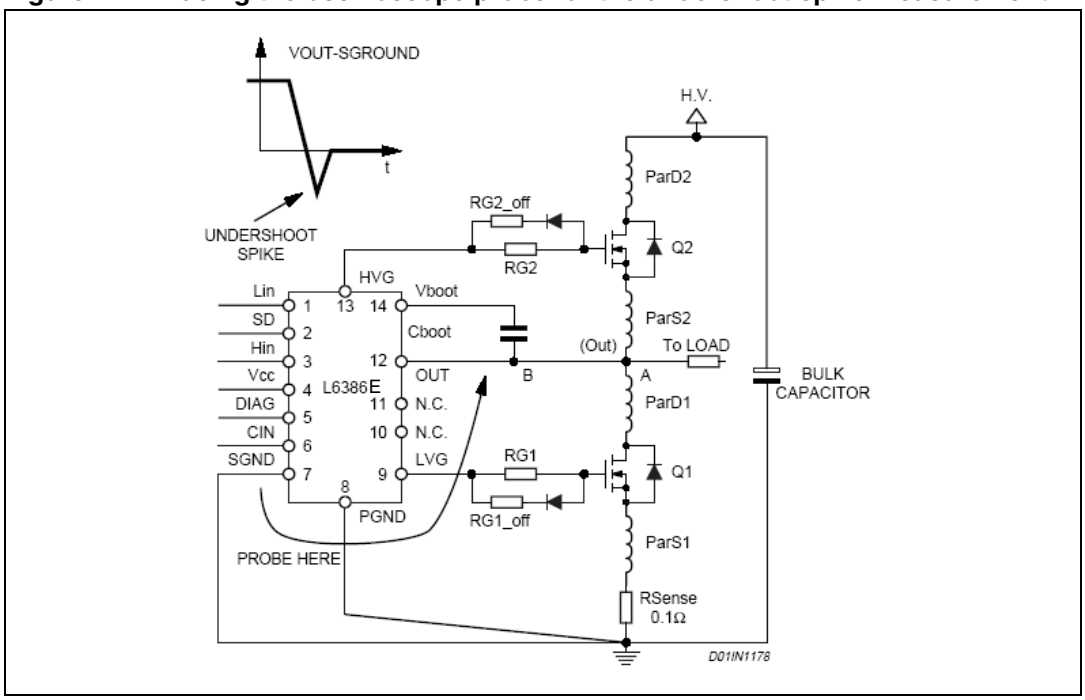
1. How to measure the below-ground spike on the OUT pin
2. The root causes of undershoot spikes
3. Dealing with undershoot spikes - tricks and layout suggestions

4.2.1 How to measure the below-ground spike on the OUT pin

It is very important to put the ground probe as close as possible to the IC signal ground pin and not to a generic ground.

If the ground probe is not well connected to a point that is close to the IC pin, a lot of noise and strange spurious spikes may be seen, due to the high current that can flow into the ground tracks of the application.

Figure 12. Placing the oscilloscope probe for the undershoot spike measurement



4.2.2 The root causes of undershoot spikes

Let's find the root causes of undershoot spikes. There are two main reasons:

1. Parasitic inductance of the tracks
2. High dI/dt values

We can use the well-known formula:

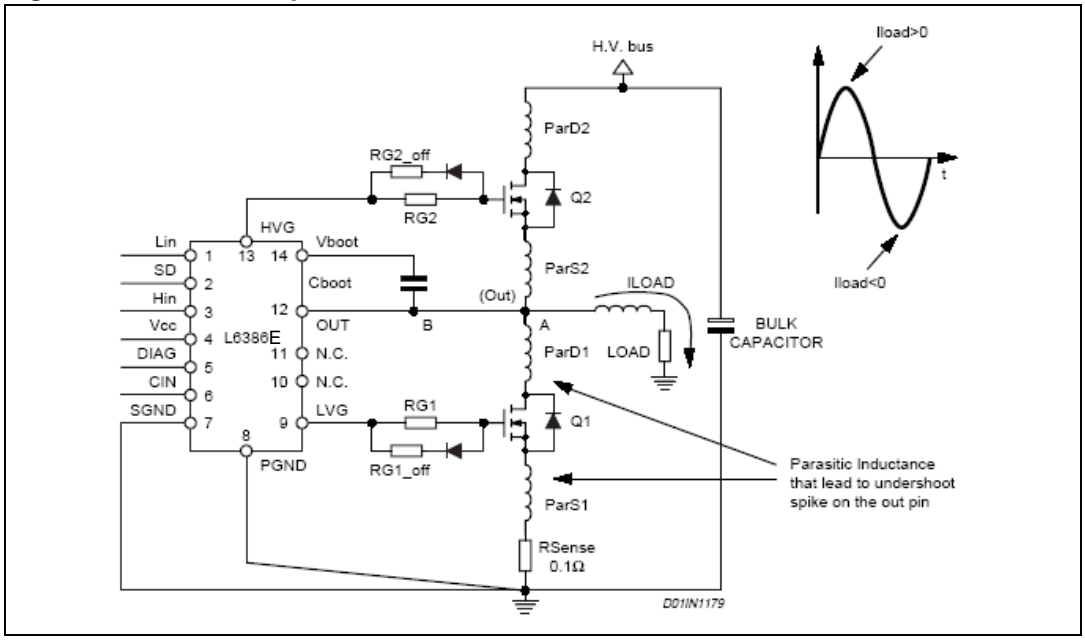
Equation 11

$$\Delta V = L \cdot \frac{dI}{dt}$$

where L = ParD1 + ParS1 (referring to *Figure 7*). Note that the parasitic inductance ParD2 and ParS2 are not involved in the path that can lead to the undershoot voltage on the OUT pin.

Let's analyze the current path during the high and low-side commutation when the direction of the load current is positive or negative (see *Figure 13*).

Figure 13. PCB trace parasitic inductance that must be minimized



- $I_{load} > 0$:
  In this condition the undershoot spike at the OUT pin appears when the high side is switched off and the load current must flow through the low-side freewheeling diode. The below-ground spike in this condition is:

Equation 12

$$V_{peak} = V_{fpk} + L \cdot \frac{dI}{dt} + (R_{sense} + R_{trace}) \cdot I_{load}$$

The peak voltage is mainly composed of the L*dI/dt and V_{fpk} contributions, all other terms are negligible. The V_{fpk} diode usually has a forward voltage around 1 V, a forward peak voltage that depends on the dI/dt current and on the diode technology. The higher the dI/dt, the higher the peak forward voltage is across the diode (*Figure 14*).

Figure 14. Diode transient forward peak voltage versus dI/dt (STTA806)

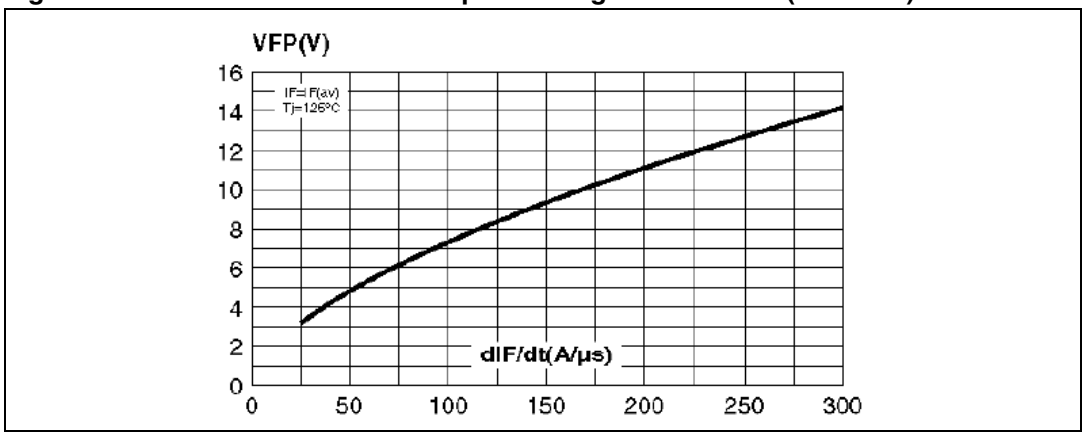


Figure 15 shows that the low side is off and the load current flows in the high-side power switch (on).

Figure 15. High side ON & low side OFF

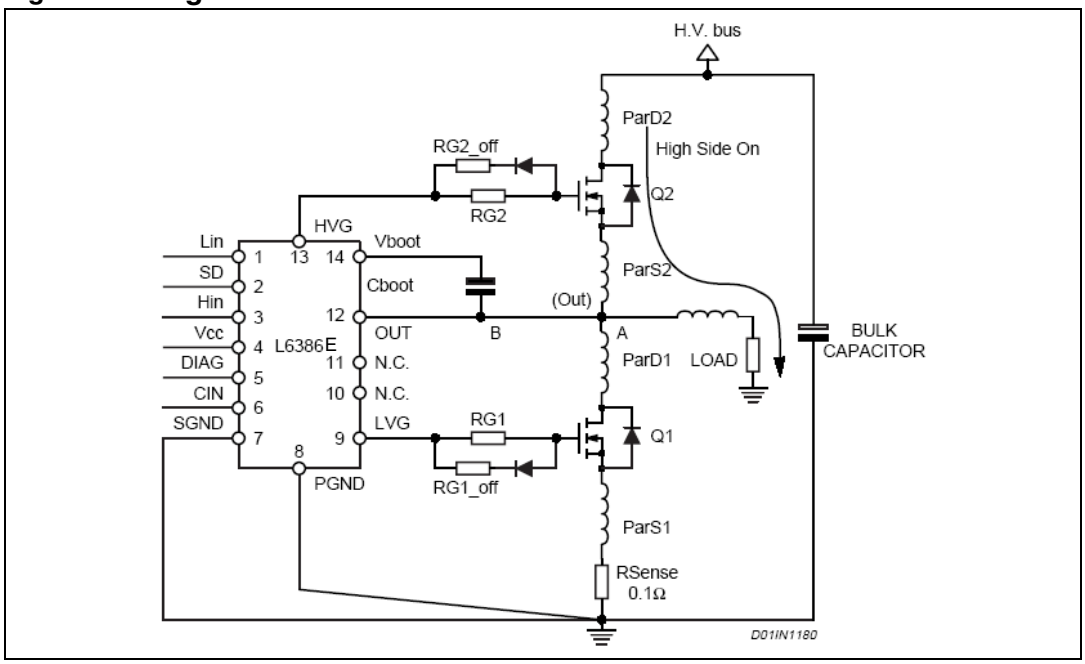
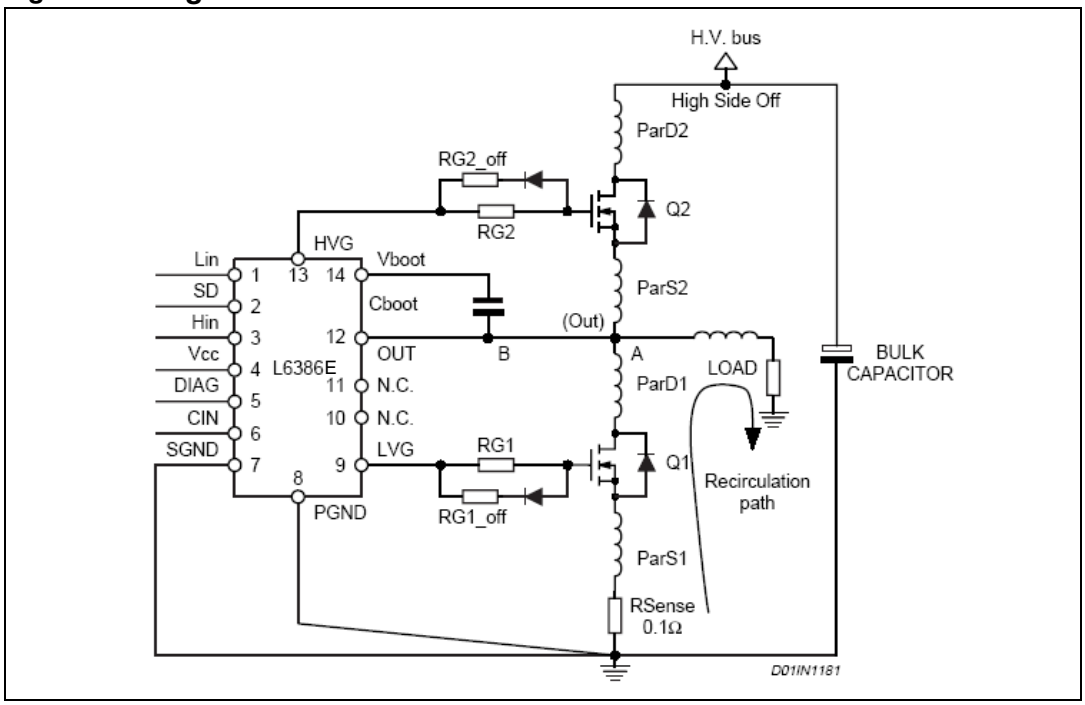


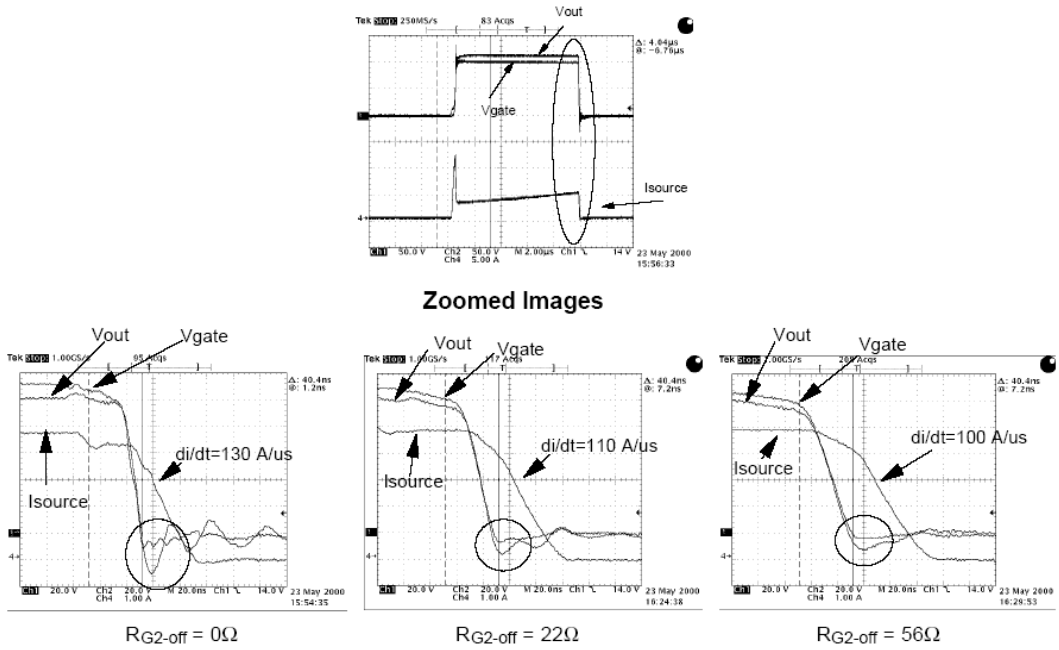
Figure 16 shows that the high side is turned off and the load current flows through the low-side freewheeling diode that is injected.

Figure 16. High side OFF & low side OFF



The oscilloscope image in *Figure 17* shows how the undershoot spike on the OUT pin is handled with the high-side turn-off resistor (Rg2_Off). Note that all the measurements shown are done with the low side always off.

Figure 17. Undershoot spike on the OUT pin



In order to reduce this undershoot voltage we can act on:

- Reducing the parasitic L between the OUT and the ground connection
- Reducing the dI/dt: this is accomplished by increasing the high-side turn-off resistor. This has the double effect of reducing the low-side diode forward peak voltage and the parasitic inductance contribution. The disadvantage is that the switching power losses increase.

During the high-side turn-on on the OUT pin we can see an overshoot spike, but in most cases this is not dangerous for the IC due to the high voltage capability of these L638xE drivers (600 V is the absolute maximum on the OUT pin).

- $I_{load} < 0$:
  In this load condition a bigger undershoot spike on the OUT pin occurs when the low-side switch is turned on during the high-side freewheeling diode conduction state. The spike is mainly related to the freewheeling diode behavior.

Figure 18 shows that the low side is off and the load current flows inside the high-side freewheeling diode.

Figure 18. High side OFF & low side OFF

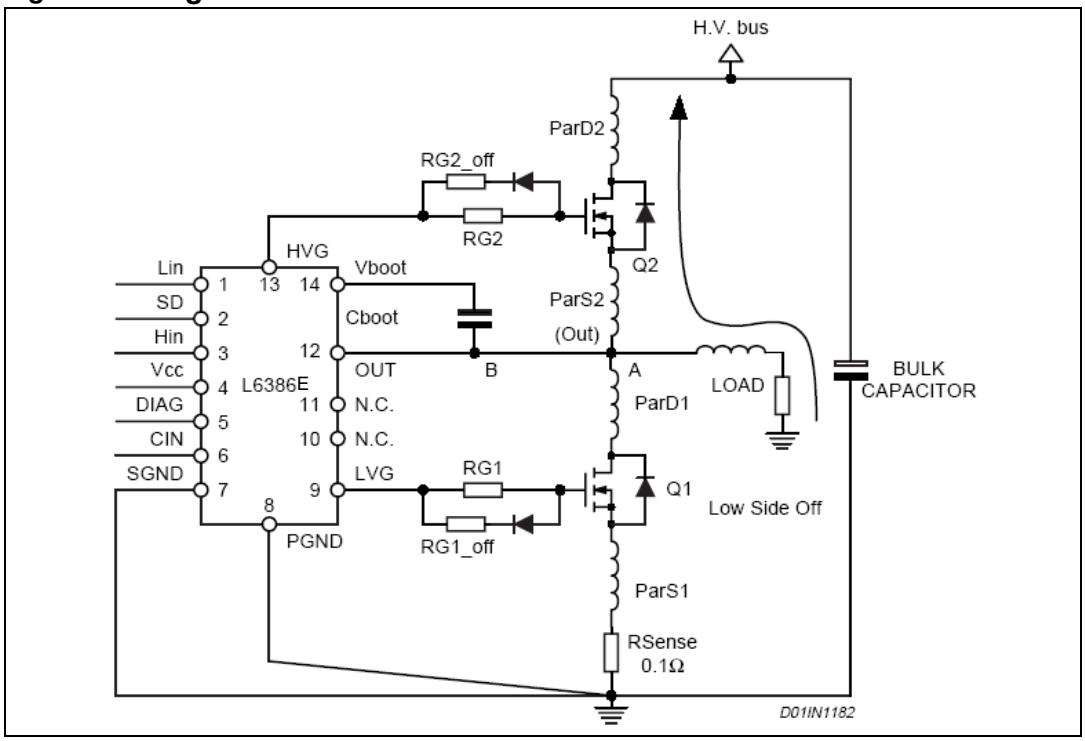


Figure 19 shows that the low side is turned on, the current that flows through the low-side switch is the sum of the charge recovered by the diode (Qrr) and the load current.

Figure 19. High side OFF & low side turned ON

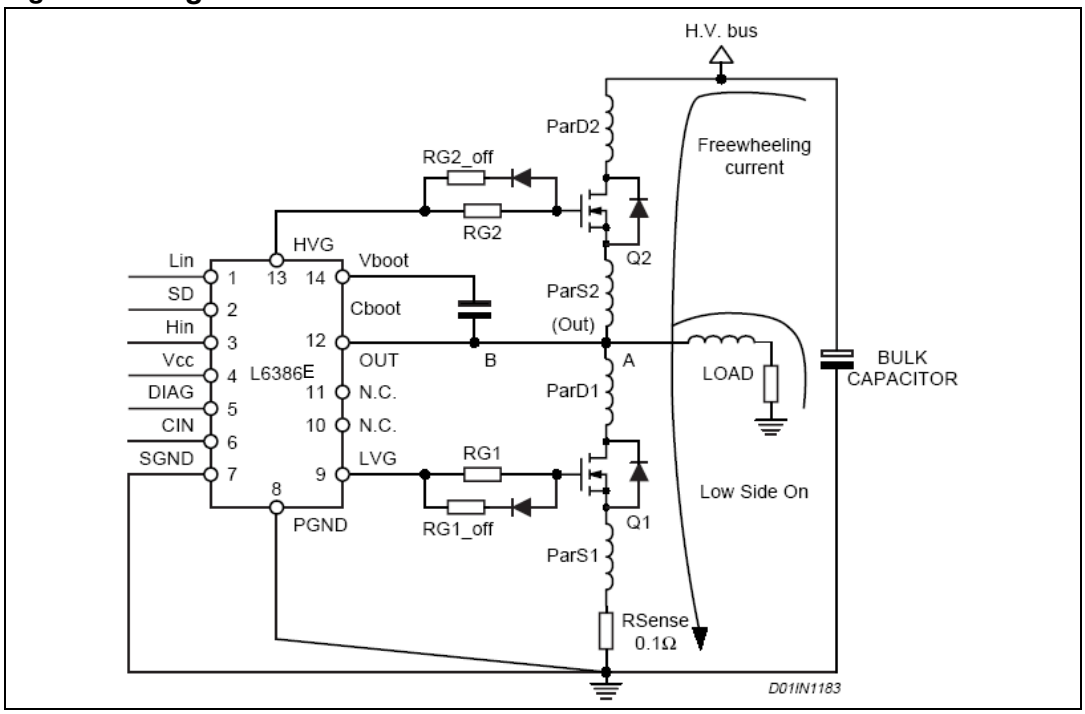


Figure 20 shows that now the high-side freewheeling diode is reverse biased and the current that flows through the low-side switch is only the load current.

Figure 20. High side OFF & low side ON

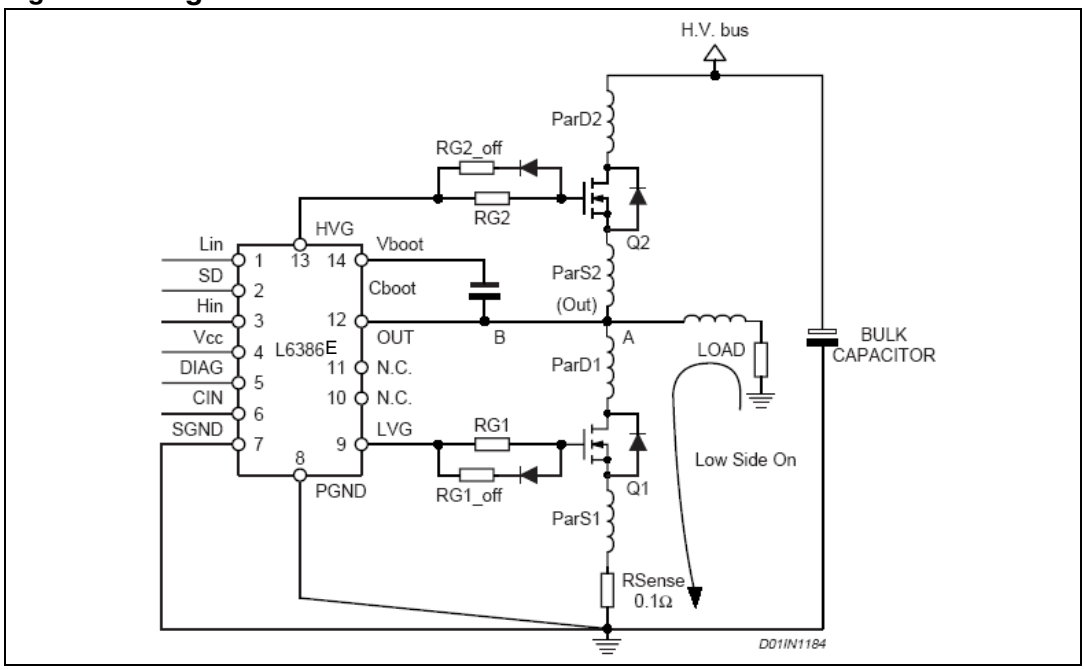
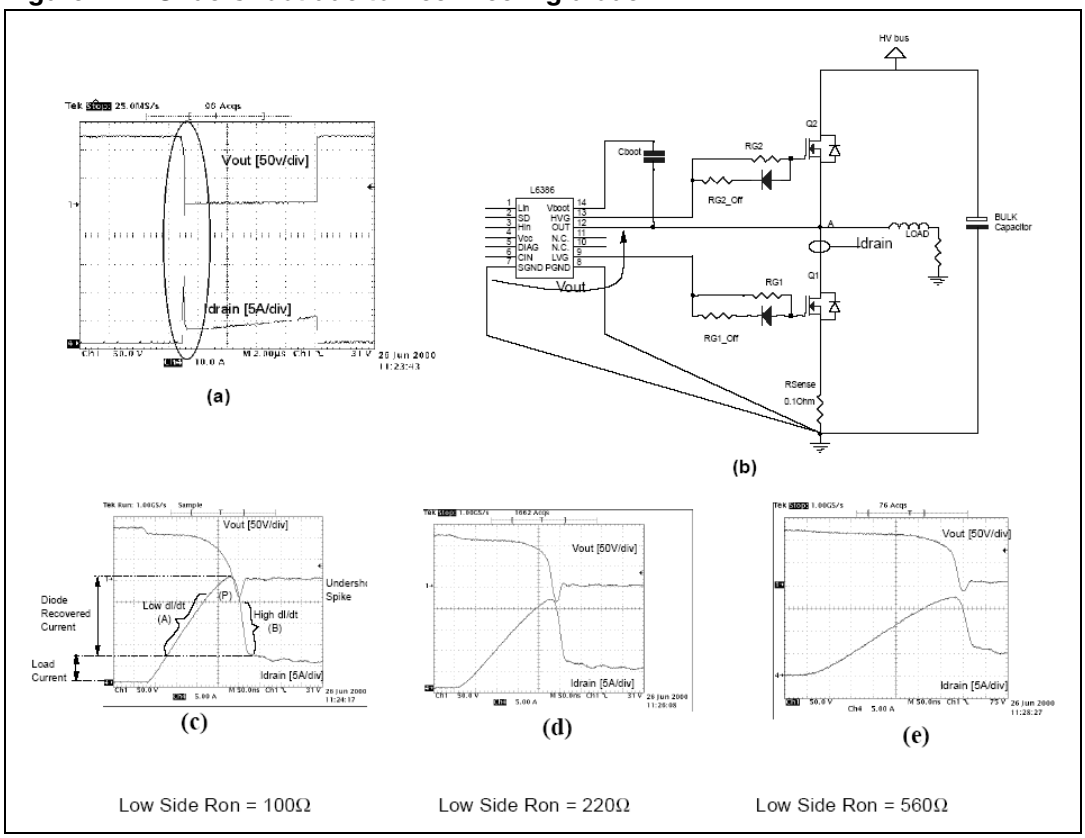


Figure 21 shows the undershoot caused by the freewheeling diode. The high-side freewheeling diode is forward biased by the load current and the low-side switch is turned on, so the current shown in the figure is the sum of the load current and the diode recovered charge.

Figure 21. Undershoot due to freewheeling diode



The picture above (*Figure 21*) shows how the high dI/dt diode recovery current leads to a below ground voltage on the OUT pin. The entire charge recovered by the high-side diode goes through the low-side switch when it turns on.The current in the low-side drain ramps up with a controlled rising slope (slope A) that is related only to the low-side turn-on speed and doesn't produce undershoot. On the other side the falling slope (slope B) is not well "limited" and it causes the undershoot spike. The high di/dt value (B) depends mainly on the diodes physical structure.

In this case the peak voltage could be reduced by acting on the PCB traces, reducing the parasitic inductance, and designing wider and shorter traces. Attention must be paid also to the diode selection. A very high value of diode-recovered current slope is very difficult to manage and forces using higher values of low-side turn-on resistance. This helps to reduce the below-ground spikes, but increases the turn-on speed and the switching losses. The turn-on resistor value should be as low as the layout allows.

For example, referring to *Figure 21* (c), if we want to limit the undershoot spike under 10 V, with the same low-side turn-on resistance, and we have 700 A/ms of dI/dt (we are talking about the second slope (B) of the current shown in the picture *Figure 21* (c)) we need a maximum parasitic inductance of 15 nH which is difficult to reach. So in this case we must increase the low-side turn-on resistance, increasing the switching losses.

The goal is to reduce the trace parasitic inductance as much as possible, but also to take into account the amount of the total freewheeling diode recovered charge and the diode softness factor.

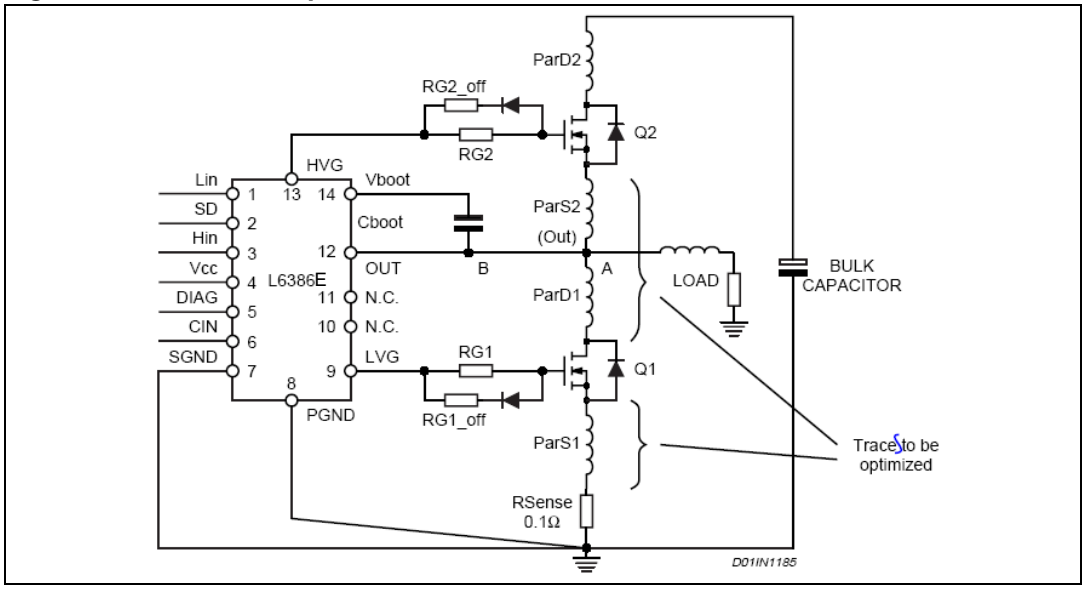
4.2.3 Tricks and layout suggestions

Layout suggestions:

The driver can easily deal with an undershoot spike in the order of -18 V (measured between the IC OUT pin and its signal ground) for a duration that must not be longer than 100 ns. The guidelines to follow in order to avoid large undershoot spike are:

- Remember that the total amount of inductance and resistance exhibited is directly proportional to the trace's length and inversely proportional to its width.
- Put both power switches of each half-bridge as close as possible in order to make traces as short and wide as possible between the low-side drain and the high-side source (this solution is aimed to minimize the stray inductance ParD1 and ParS2 shown in *Figure 22*).
- Pay attention to the traces between the low-side source, the sense resistor, and the power ground reference, making them shorter and wider (to reduce ParS1, *Figure 22*). Remember that all load current flows in this path.

Figure 22. Path to be optimized

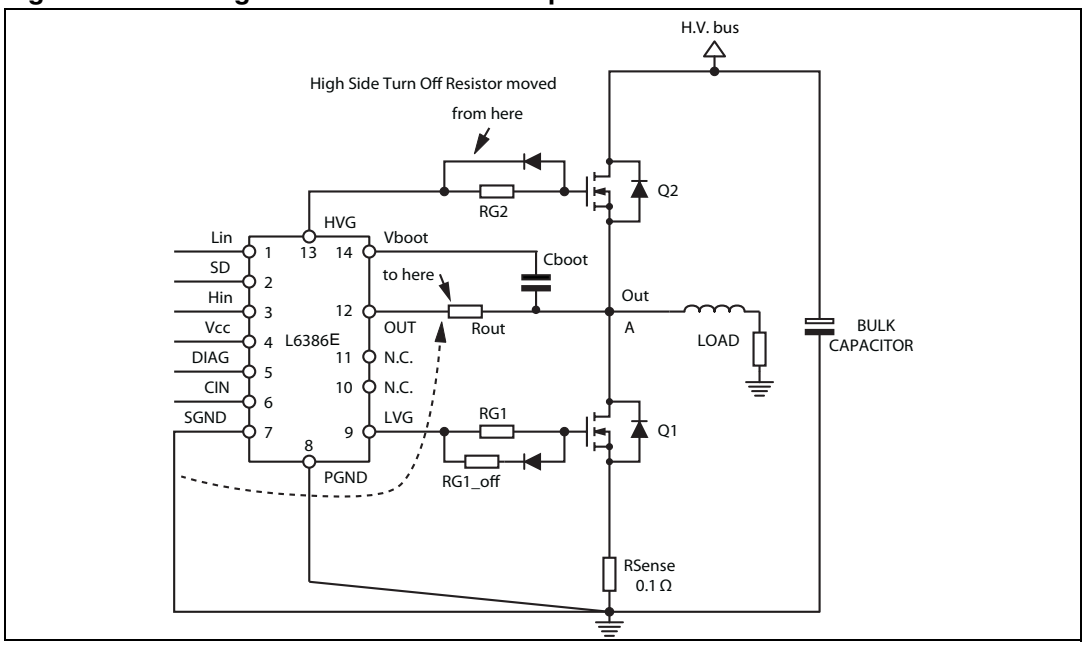


- Use "inductance free" sense resistors
- Shorten the power switch lead length

Tricks

- If we are not able to reduce the below-ground spikes acting only on the layout, a resistor in series to the OUT pin (as indicated in *Figure 23*) is a good trick that improves the device immunity. The resistor is not additional, the part count does not change, but it is the high side turn-off resistor that is moved on the OUT pin. In this way we can deal with undershoot spikes exceeding -18 V.

Figure 23. Placing resistance on the OUT pin

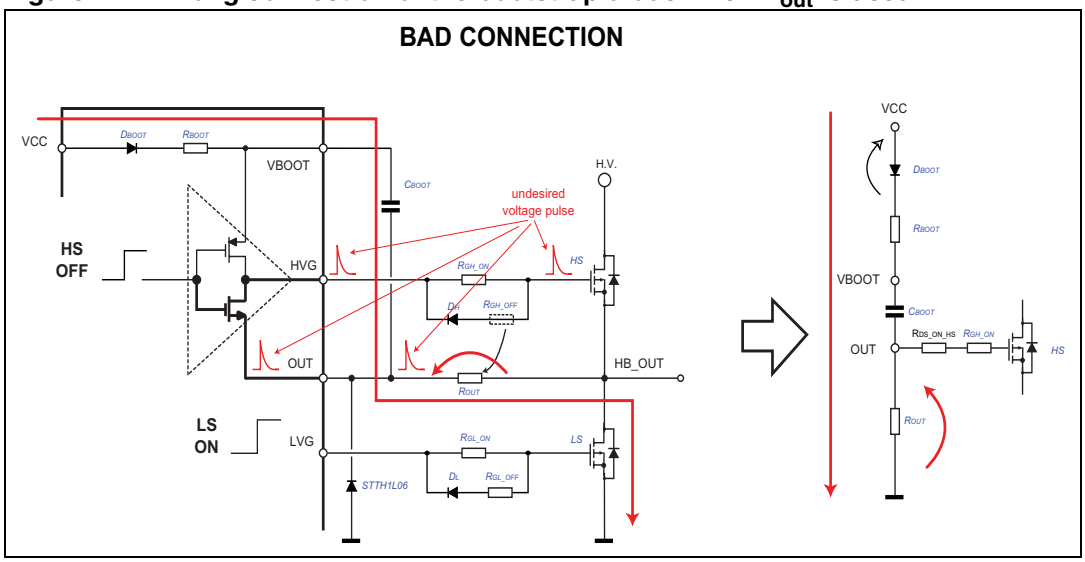


This resistor, having values between 10-22 Ω, is not mandatory for the application, but helps to manage heavy below-ground spikes. This limits below ground voltage perceived by the OUT pin and improves the spike device immunity.

We strictly suggest avoiding high resistor values, because the resistor is in series with the bootstrap capacitor charging path.

When the output resistor is used, some important design rules should be considered. First of all the negative terminal of the bootstrap capacitor must be connected between the R_{out} resistor and the output node of the half-bridge and not between the OUT pin of the gate driver and the R_{out} resistor. The main reason is well illustrated in *Figure 24*.

Figure 24. Wrong connection of the bootstrap diode when R_{out} is used

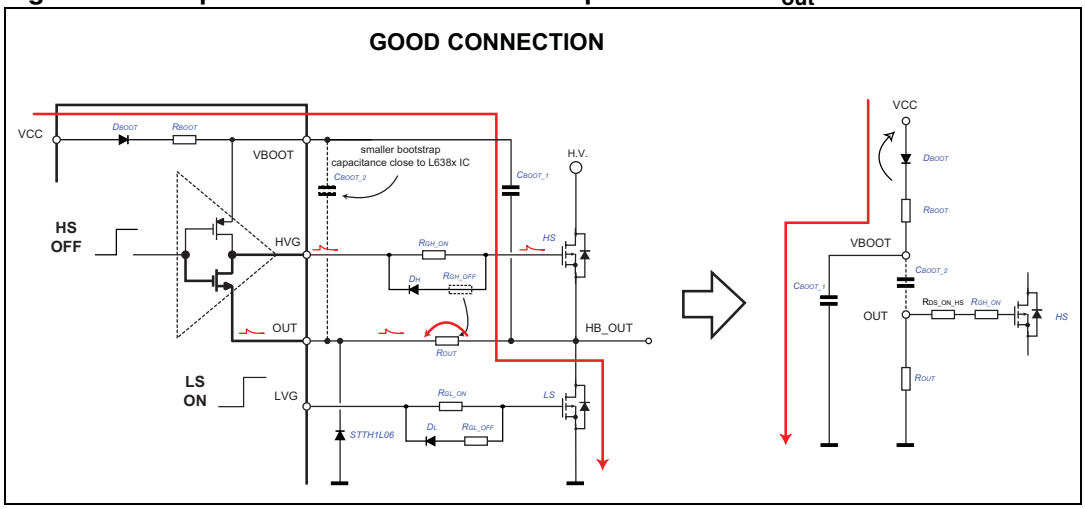


At application power-up usually the low side is turned on to charge the bootstrap capacitor that is uncharged. Therefore a rush current flows from the bootstrap diode

through the capacitor, the R_{out} resistor and the low-side switch towards ground. Moreover, during this phase, the HVG output of the gate driver is set to low level (to keep the high-side switch well turned off) and the impedance between HVG pin and OUT pin is very low (some Ω). This low impedance path directly transfers the voltage drop due to the flow of the bootstrap charge current through the R_{out} resistor on the HVG pin. This undesired pulse could cause a brief but dangerous turn-on of the high-side power switch while the low-side switch is ON, causing cross-conduction in the half-bridge. This condition clearly must be avoided. The maximum value of the pulse amplitude is the voltage partition of the V_{CC}-V_{diode} between the R_{out} and the R_{out}, while the time constant (referred to the OUT pin) depends on the product between C_{boot} and R_{out}+R_{boot}.

The correct connection is provided in *Figure 25*.

Figure 25. Proper connection of the bootstrap diode when R_{out} is used



The negative terminal of the bootstrap capacitor is connected directly on the output of the half-bridge. In this way the rush current for the bootstrap charge does not flow through the R_{out} resistor and no undesired pulses are transferred to the gate of the power MOSFET (or IGBT). Sometimes when R_{out} is used, it is possible to place a small bootstrap capacitor C_{boot2} close to the L638xE IC directly on the IC driver pins OUT and V_{boot}. This capacitor is useful for noise filtering of the high-side voltage supply. Consider that the value of this capacitor must be kept low in order to avoid the issue of the HVG pulse described in *Figure 25*, considering the voltage partition of the charging network.

For the same reason, wherever an external diode is used, it is strongly recommended to reduce the bootstrap charge spike by placing in series to the external diode a further resistor R_{boot}.

- Another way to reduce the below-ground spike is to slow down the switching speed by means of the gate resistor. When increasing the high-side turn-off series resistor the negative spikes amplitude decrease, as shown in *Figure 17*.
- Pay attention when selecting the freewheeling diodes as high values in terms of recovered charge can lead to a high value of dI/dt and then to spikes below ground on the OUT pin (*Figure 21*).The only way to control this dI/dt is by increasing the low-side turn-on time by means of the turn-on resistor, but this leads also to an increase in terms of switching losses.

Further suggestion:

- The layout must also optimize the gate drive loops in order to improve mainly the power switch turn-on immunity. High dV/dt values between the power switch drain-source inject current inside the gate drive path via the drain-gate capacitance. This impulsive current must be absorbed by the driver. But if the gate drive loop is not well optimized and has a long and thin trace, the parasitic inductance can lead to the power switch turn-on. This is called "induced turn-on".

Figure 26. Gate drive loops which have to be optimized

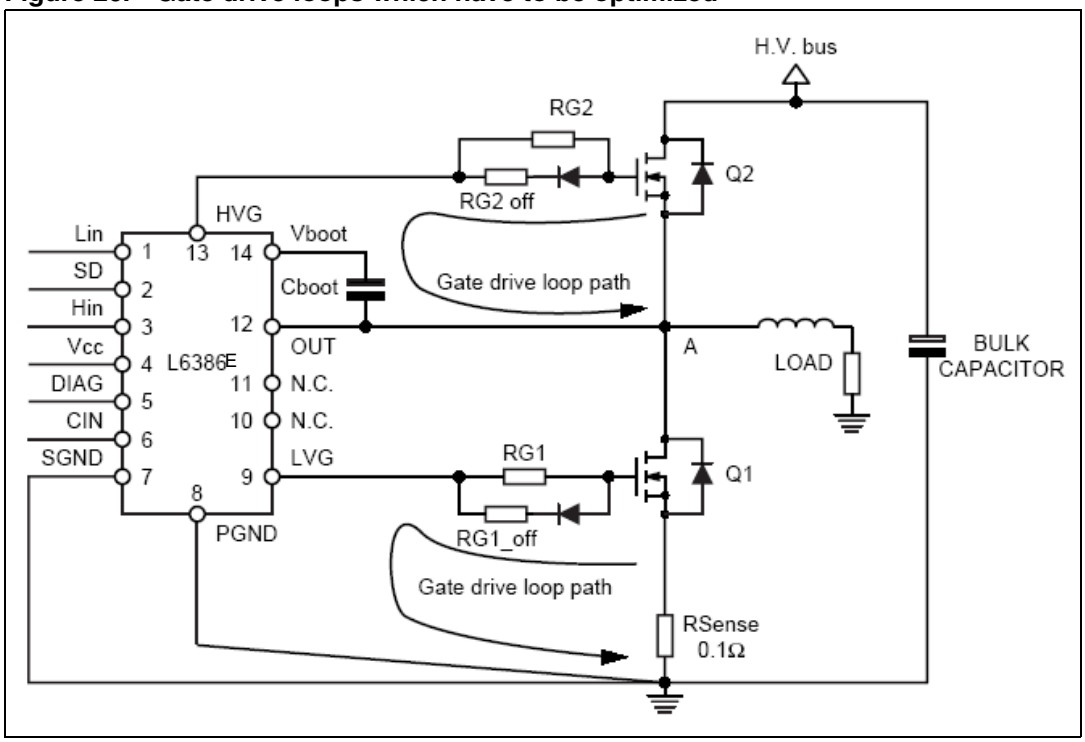
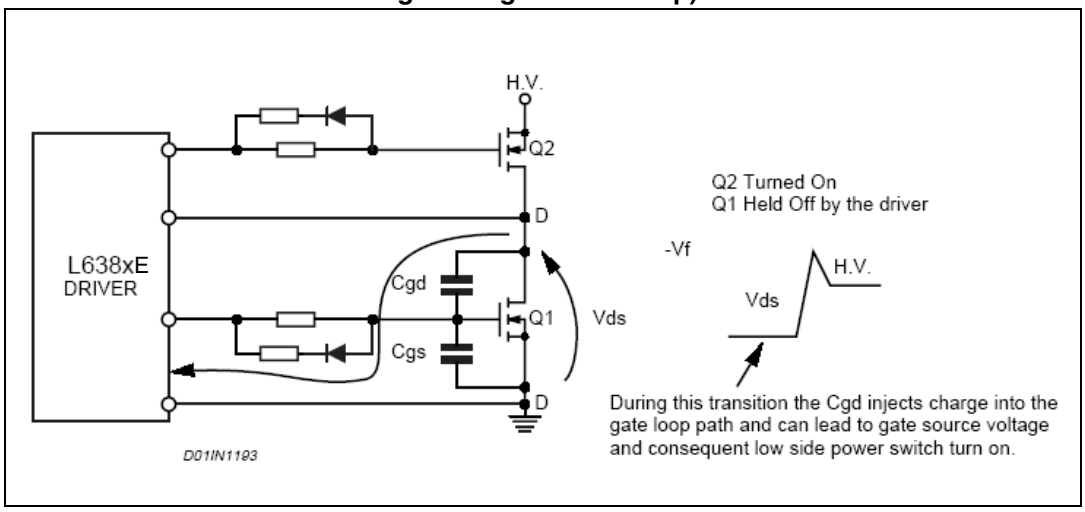


Figure 27. Current injected inside the low-side gate drive loop (the same concept is also valid for the high-side gate drive loop)

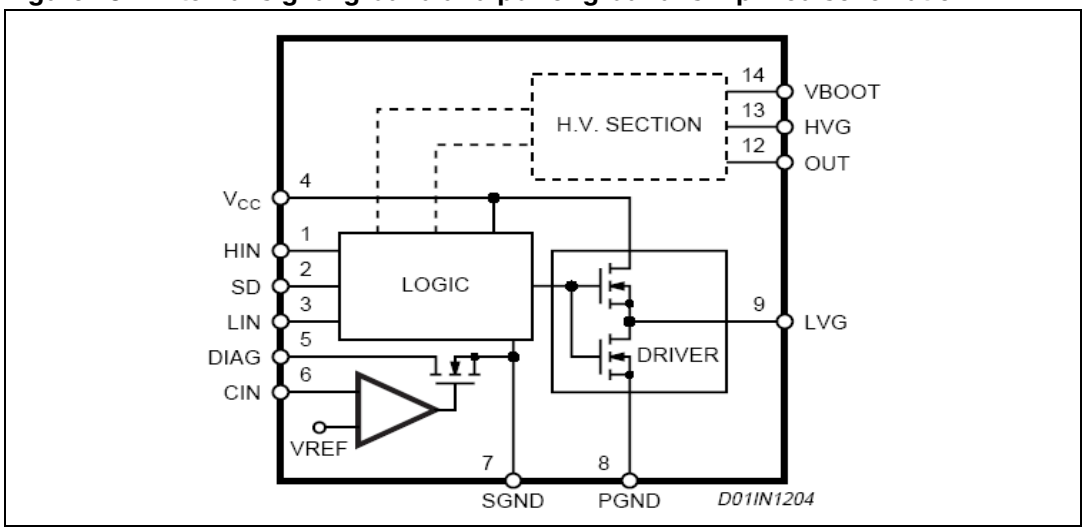


5 How to deal with signal ground and power ground

Inside the L638xE family the L6386E has two ground connections:

- Power ground: reference for internal low-side power driver. On this ground the low-side gate loop's current circulates.
- Signal ground: reference for all the internal logic. On this reference only the logic supply current flows.

Figure 28. Internal signal ground and power ground: simplified schematic



Two different grounds avoid that the gate drive current flows on signal ground, leading to internal ground noise.

Control ground is extremely sensitive and separated grounds help to avoid that noise generated from the low-side turn-off gate drive current reaches the internal logic section. Noise generated on this signal ground remains inside the device and affects the functioning of the IC.

We can suggest two different ways to connect these ground references:

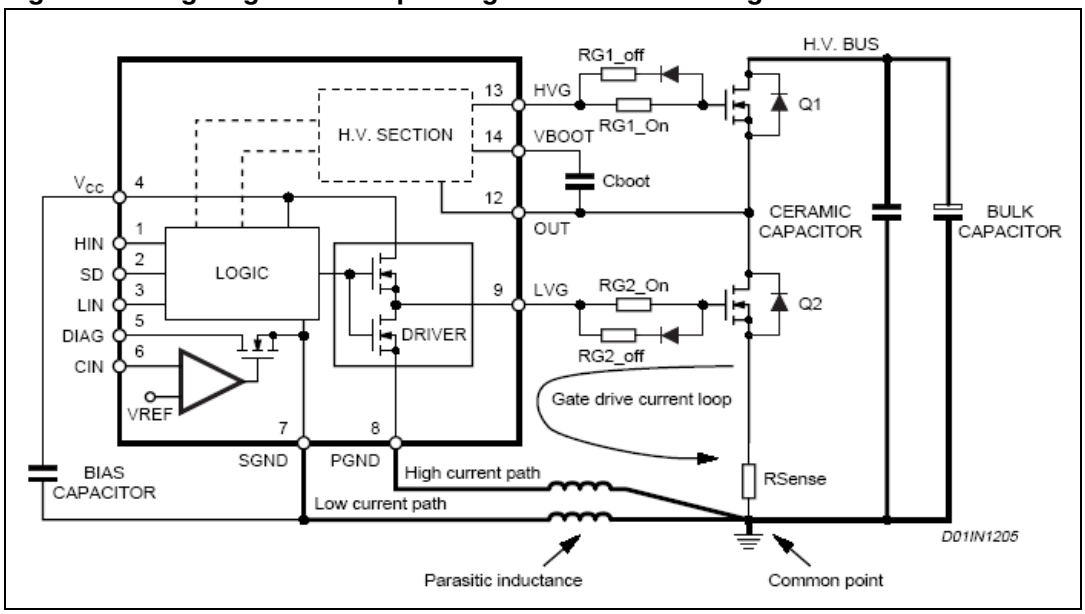
1. Signal and power ground connected together (suggested solution)
2. Signal and power ground separated

Let's analyze both solutions.

5.1 Signal and power ground connected together

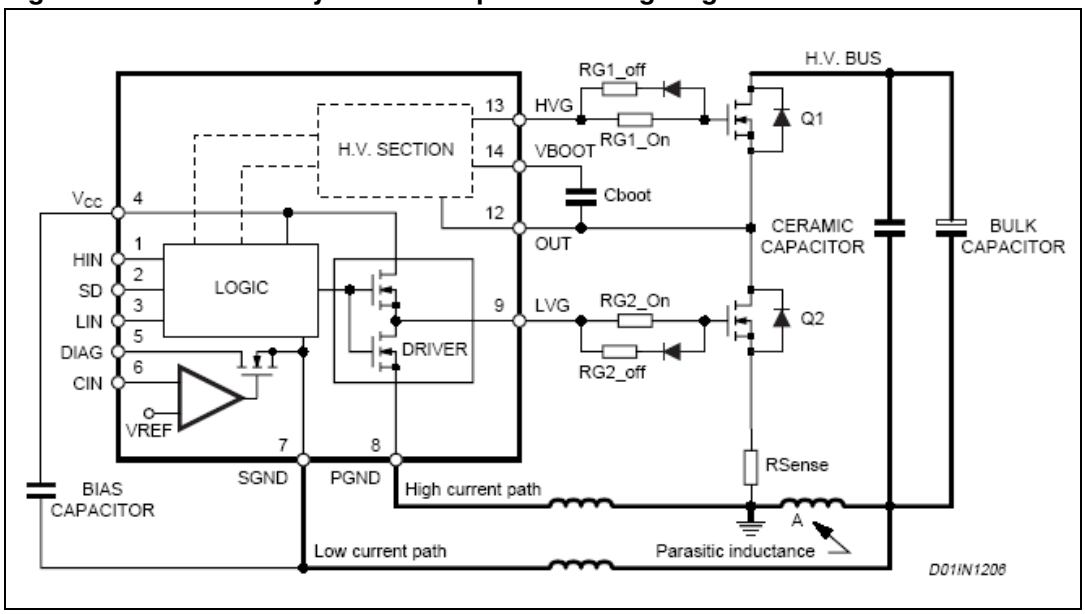
The connection between the two grounds is done in a specific point: the common end of the current sense resistor. This point must be filtered with an electrolytic capacitor connected between ground and the high-voltage bus. A high-voltage ceramic capacitor connected in parallel with the electrolytic one is also advisable which helps to reduce the equivalent ESR and to smooth the high-frequency voltage transient.

Figure 29. Signal ground and power ground connected together



- Advantages:
  - The solution proposed helps to limit the noise seen by the signal ground due to the low-side turn-off gate current. This current flows on the path highlighted in *Figure 29*. Voltage transient on the power ground pin due to parasitic inductance is not seen on signal ground. Remember that the turn-off gate current can be up to 650 mA and can lead to heavy spikes on the IC power ground.
  - Differential voltage between signal and power ground is minimized and due only to the low-side gate drive current. There is no DC voltage between the two grounds but only transient voltage during the low-side switch turn-off. It is important to limit the transient voltage below ground on the PGND to avoid internal power drive damages.
- Disadvantage:
  - PCB layout of the low-side gate drive loop could be too "long". If it is not done well, the parasitic inductance and resistance could be non-negligible. This means that we need to make shorter and wider traces in order to minimize all the parasitic elements and improve the power switch "induced turn-on" immunity. *Figure 30* shows an incorrect way to connect signal and power ground because all the load current flows on the parasitic inductance inside the trace A and can lead to high differential voltage between the two grounds.

Figure 30. Incorrect way to connect power and signal ground



In a three-phase motor control three half-bridges must be used. The ground's common point for all three sections is highlighted in *Figure 29*. Signal and power grounds must be connected at this point with a low inductive path (especially for the power ground connection).

5.2 Signal and power ground separated

In this solution (*Figure 31*), power ground is connected to the low-side source and the sense resistor is outside the gate drive loop. The turn-off resistor is moved from the low-side gate to the "power ground-source path" as shown in *Figure 31*. The resistor limits the current absorbed from the power ground when the voltage goes below the signal ground.

The values suggested are the same that are also used for the turn-off resistor: in the range of 10-100 Ω, or anyway more than 10 Ω.

- Advantages:
  - Noise seen by signal ground due the low-side turn-off gate current is limited (as previously stated for the first solution)
  - Low-side gate drive loop is shorter if compared to the first solution (because the sense resistor is outside of this loop).
- Disadvantages:
  - Differential voltage between the two grounds is proportional to the load current (see *Figure 32* and *33*). Transient and DC voltage differences could be high which leads to device damage. In order to avoid IC failure, putting the low-side turn-off resistor on the path shown in *Figure 31* is mandatory. This limits the current absorbed from the power ground when its voltage goes below the signal ground.

Figure 31. Power ground connected to the low-side source

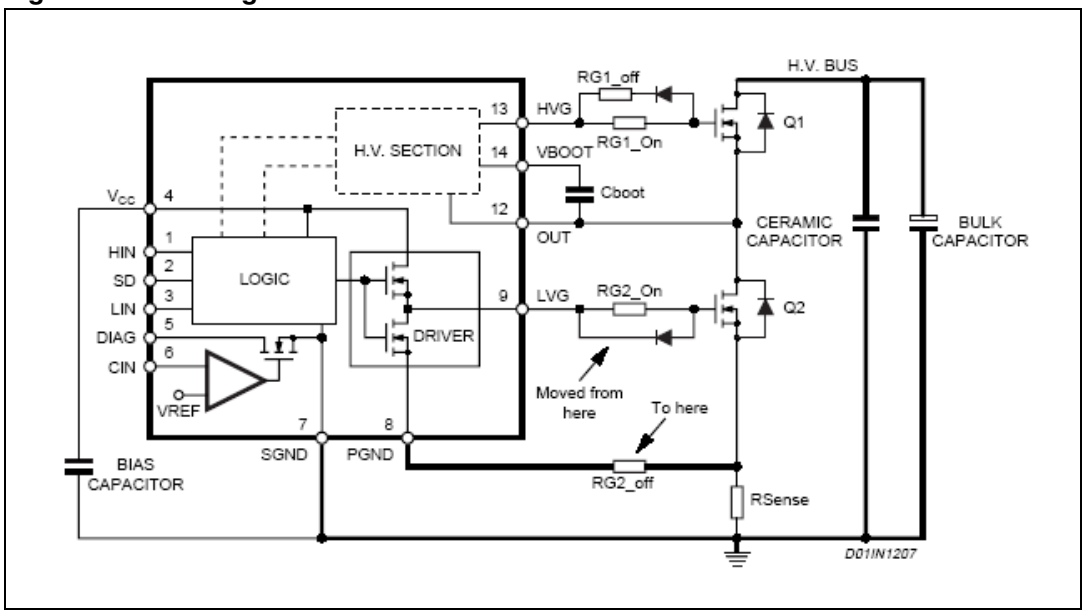


Figure 32. Voltage between power and signal ground (load current flowing out of the bridge)

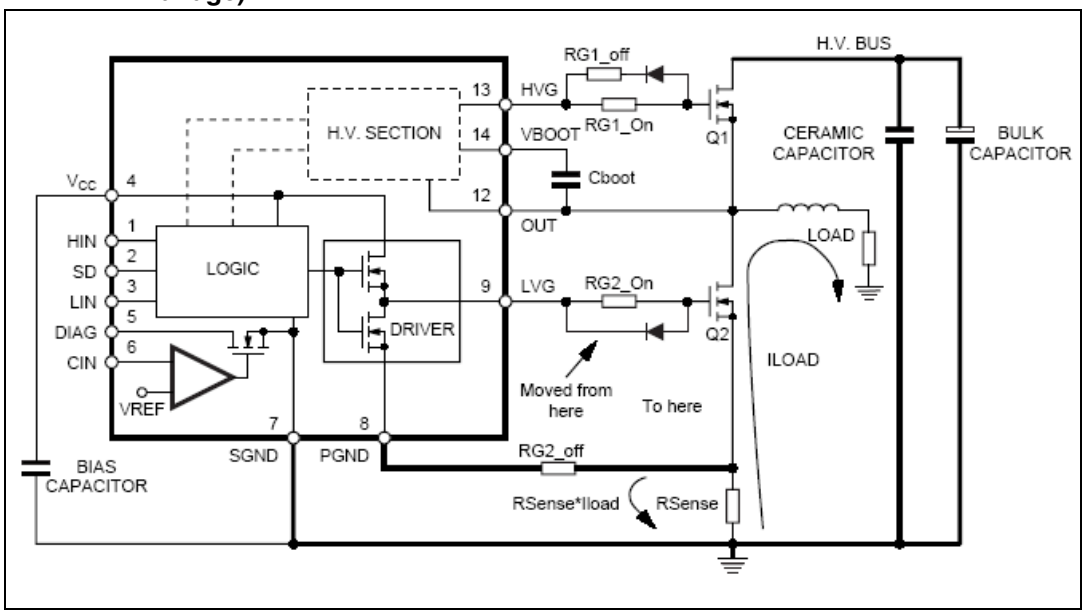
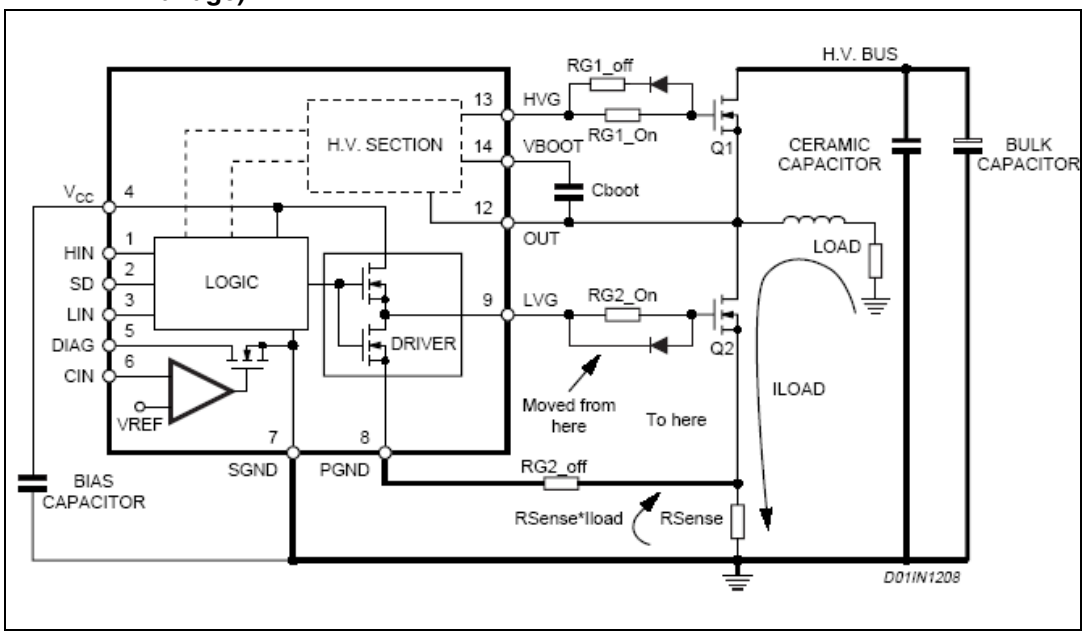


Figure 33. Voltage between power and signal ground (load current flowing into the bridge)



6 Revision history

Table 1. Document revision history

Date	Revision	Changes
21-Jun-2004	2	Minor text changes
01-Aug-2008	3	– Document reformatted. No content change – Updated *Section : Tricks* – L6384 replaced by L6384E, L6385 replaced by L6385E, L6386 replaced by L6386E, L6387 replaced by L6387E, L6388 replaced by L6388E, L638x replaced by L638xE