**Introduction**

This application note describes the I2C protocol used in the STM32 microcontroller bootloader, detailing each supported command.

This document applies to the STM32 products embedding bootloader versions V5.x, V6.x, V7.x, V8.x, V9.x, V10.x, V11.x and V13.x, as specified in the application note AN2606 “STM32 microcontroller system memory boot mode”, available on www.st.com. These products are listed in Table 1, and are referred to as STM32 throughout the document.

For more information about the I2C hardware resources and requirements for your device bootloader, refer to the already mentioned AN2606.

---

**Table 1. Applicable products**

<table>
<thead>
<tr>
<th>Type</th>
<th>Part numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontrollers</td>
<td>STMicroelectronics:</td>
</tr>
<tr>
<td></td>
<td>– STM32F0 Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32F030xC, STM32F04xxx, STM32F07xxx, STM32F09xxx</td>
</tr>
<tr>
<td></td>
<td>– STM32F3 Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32F303xx, STM32F318xx, STM32F328xx, STM32F334xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32F358xx, STM32F378xx, STM32F398xx</td>
</tr>
<tr>
<td></td>
<td>– STM32F4 Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32F401xx, STM32F405xx, STM32F407xx, STM32F410xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32F411xx, STM32F412xx, STM32F415xx, STM32F417xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32F427xx, STM32F429xx, STM32F437xx, STM32F439xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32F446xx, STM32F469xx, STM32F479xx</td>
</tr>
<tr>
<td></td>
<td>– STM32F7 Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32F722xx, STM32F723xx, STM32F732xx, STM32F733xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32F745xx, STM32F746xx, STM32F756xx, STM32F765xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32F767xx, STM32F769xx, STM32F777xx, STM32F779xx</td>
</tr>
<tr>
<td></td>
<td>– STM32G0 Series</td>
</tr>
<tr>
<td></td>
<td>– STM32G4 Series</td>
</tr>
<tr>
<td></td>
<td>– STM32H7 Series</td>
</tr>
<tr>
<td></td>
<td>– STM32L0 Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32L07xxx, STM32L08xxx</td>
</tr>
<tr>
<td></td>
<td>– STM32L4 Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32L431xx, STM32L432xx, STM32L433xx, STM32L442xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32L443xx, STM32L471xx, STM32L475xx, STM32L476xx,</td>
</tr>
<tr>
<td></td>
<td>– STM32L486xx, STM32L496xx, STM32L4A6xx</td>
</tr>
<tr>
<td></td>
<td>– STM32L5 Series</td>
</tr>
<tr>
<td></td>
<td>– STM32WB Series:</td>
</tr>
<tr>
<td></td>
<td>– STM32WB50CG, STM32WB55xx</td>
</tr>
</tbody>
</table>
Contents

1  I2C bootloader code sequence ............................................. 5

2  Bootloader command set ..................................................... 6
   2.1 Get command ............................................................ 8
   2.2 Get Version command ................................................ 11
   2.3 Get ID command ....................................................... 12
   2.4 Read Memory command ................................................ 14
   2.5 Go command ............................................................ 17
   2.6 Write Memory command ............................................... 20
   2.7 Erase Memory command ............................................... 23
   2.8 Write Protect command ............................................... 26
   2.9 Write Unprotect command ........................................... 29
   2.10 Readout Protect command .......................................... 30
   2.11 Readout Unprotect command ...................................... 32
   2.12 No-Stretch Write Memory command ................................ 34
   2.13 No-Stretch Erase Memory command ................................ 37
   2.14 No-Stretch Write Protect command ................................. 40
   2.15 No-Stretch Write Unprotect command .............................. 43
   2.16 No-Stretch Readout Protect command .............................. 45
   2.17 No-Stretch Readout Unprotect command ............................ 47

3  Bootloader protocol version evolution ................................. 49

4  Revision history ............................................................. 50
List of tables

Table 1. Applicable products ................................................................. 1
Table 2. I2C bootloader commands ......................................................... 6
Table 3. Bootloader protocol versions ....................................................... 49
Table 4. Document revision history ......................................................... 50
List of figures

Figure 1. Bootloader for STM32 with I2C ......................................................... 5
Figure 2. Get command: host side ................................................................. 8
Figure 3. Get command: device side .............................................................. 9
Figure 4. Get Version: host side ................................................................. 11
Figure 5. Get Version: device side .............................................................. 12
Figure 6. Get ID command: host side ......................................................... 13
Figure 7. Get ID command: device side ...................................................... 13
Figure 8. Read Memory command: host side ............................................. 15
Figure 9. Read Memory command: device side ......................................... 16
Figure 10. Go command: host side ............................................................ 18
Figure 11. Go command: device side ........................................................ 19
Figure 12. Write Memory command: host side ......................................... 21
Figure 13. Write Memory command: device side ..................................... 22
Figure 14. Erase Memory command: host side ....................................... 24
Figure 15. Erase Memory command: device side .................................... 25
Figure 16. Write Protect command: host side ........................................ 27
Figure 17. Write Protect command: device side ..................................... 28
Figure 18. Write Unprotect command: host side ..................................... 29
Figure 19. Write Unprotect command: device side .................................. 30
Figure 20. Readout Protect command: host side ..................................... 31
Figure 21. Readout Protect command: device side .................................. 31
Figure 22. Readout Unprotect command: host side ................................ 32
Figure 23. Readout Unprotect command: device side ................................ 33
Figure 24. No-Stretch Write Memory command: host side ..................... 35
Figure 25. No-Stretch Write Memory command: device side .................. 36
Figure 26. No-Stretch Erase Memory command: host side ..................... 38
Figure 27. No-Stretch Erase Memory command: device side .................. 39
Figure 28. No-Stretch Write Protect command: host side ....................... 41
Figure 29. No-Stretch Write Protect command: device side .................... 42
Figure 30. No-Stretch Write Unprotect command: host side .................... 43
Figure 31. No-Stretch Write Unprotect command: device side ................ 44
Figure 32. No-Stretch Readout Protect command: host side ................... 45
Figure 33. No-Stretch Readout Protect command: device side ................ 46
Figure 34. No-Stretch Readout Unprotect command: host side ................ 47
Figure 35. No-Stretch Readout Unprotect command: device side ............ 48
1 I2C bootloader code sequence

The I2C bootloader code sequence for STM32 microcontrollers, based on Arm® core(s) is sketched in Figure 1.

Figure 1. Bootloader for STM32 with I2C

Note: The I2C slave address for each product bootloader is specified in the AN2606.

Once the system memory boot mode has been entered and the STM32 microcontroller has been configured (for more details, refer to your STM32 system memory boot mode application note), the bootloader code begins to scan the I2C_SDA line pin, waiting to detect its own address on the bus. Once detected, the I2C bootloader firmware begins receiving host commands.

---

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
2 Bootloader command set

“No-Stretch” commands are supported starting from V1.1 protocol version and enable a better management of commands when the Host has to wait for a significant time before operation is accomplished by bootloader.

It is recommended to use the “No-Stretch” commands instead of equivalent regular commands whenever possible.

The supported commands are listed in Table 2.

<table>
<thead>
<tr>
<th>Commands(1)</th>
<th>Command code</th>
<th>Command description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Get(2)</td>
<td>0x00</td>
<td>Gets the version and the allowed commands supported by the current version of the bootloader</td>
</tr>
<tr>
<td>Get Version(2)</td>
<td>0x01</td>
<td>Gets the bootloader version</td>
</tr>
<tr>
<td>Get ID(2)</td>
<td>0x02</td>
<td>Gets the chip ID</td>
</tr>
<tr>
<td>Read Memory</td>
<td>0x11</td>
<td>Reads up to 256 bytes of memory, starting from an address specified by the application</td>
</tr>
<tr>
<td>Go(3)</td>
<td>0x21</td>
<td>Jumps to user application code located in the internal Flash memory</td>
</tr>
<tr>
<td>Write Memory(3)</td>
<td>0x31</td>
<td>Writes up to 256 bytes to the memory, starting from an address specified by the application</td>
</tr>
<tr>
<td>No-Stretch Write Memory(3)(4)</td>
<td>0x32</td>
<td>Writes up to 256 bytes to the memory, starting from an address specified by the application and returns busy state while operation is ongoing</td>
</tr>
<tr>
<td>Erase</td>
<td>0x44</td>
<td>Erases from one to all Flash memory pages or sectors using two-byte addressing mode</td>
</tr>
<tr>
<td>No-Stretch Erase(3)(4)</td>
<td>0x45</td>
<td>Erases from one to all Flash memory pages or sectors using two-byte addressing mode and returns busy state while operation is ongoing</td>
</tr>
<tr>
<td>Write Protect</td>
<td>0x63</td>
<td>Enables write protection for some sectors</td>
</tr>
<tr>
<td>No-Stretch Write Protect(4)</td>
<td>0x64</td>
<td>Enables write protection for some sectors and returns busy state while operation is ongoing</td>
</tr>
<tr>
<td>Write Unprotect</td>
<td>0x73</td>
<td>Disables write protection for all Flash memory sectors</td>
</tr>
<tr>
<td>No-Stretch Write Unprotect(4)</td>
<td>0x74</td>
<td>Disables write protection for all Flash memory sectors and returns busy state while operation is ongoing</td>
</tr>
<tr>
<td>Readout Protect</td>
<td>0x82</td>
<td>Enables read protection</td>
</tr>
<tr>
<td>No-Stretch Readout Protect(4)</td>
<td>0x83</td>
<td>Enables read protection and returns busy state while operation is ongoing</td>
</tr>
<tr>
<td>Readout Unprotect(2)</td>
<td>0x92</td>
<td>Disables read protection</td>
</tr>
<tr>
<td>No-Stretch Readout Unprotect(2)(4)</td>
<td>0x93</td>
<td>Disables read protection and returns busy state while operation is ongoing</td>
</tr>
</tbody>
</table>

1. If a denied command is received, or if an error occurs during the command execution, the bootloader sends a NACK byte and goes back to command checking.
No-Stretch commands

No-Stretch commands make it possible to execute Write, Erase, Write Protect, Write Unprotect, Read Protect and Read Unprotect operations without stretching I2C line while the bootloader is performing the operation. It is possible to communicate with other devices on the bus while the bootloader performs operations that require waiting time.

The difference between these commands and the standard ones is at the end of the command: when Host requests ACK/NACK at the end of the command, instead of stretching the I2C line, the bootloader answers with a third state, which is Busy (0x76). When Host receives Busy state, it polls again on the state and reads one byte till it receives ACK or NACK response.

Communication safety

All communications from the programming host to the device are verified by checksum. Received blocks of data bytes are XOR-ed. A byte containing the computed XOR of all previous bytes is added to the end of each communication (checksum byte). By XOR-ing all received bytes, data plus checksum, the result at the end of the packet must be 0x00.

For each command, the host sends a byte and its complement (XOR = 0x00).

Each packet is either accepted (ACK answer) or discarded (NACK answer):
- ACK = 0x79
- NACK = 0x1F

With No-Stretch commands Busy state is sent instead of ACK or NACK when an operation is ongoing:
- BUSY = 0x76

Note: The host frame can be one of the following:
- Send Command frame: The host initiates communication as master transmitter, and sends two bytes to the device: command code + XOR.
- Wait for ACK/NACK frame: The host initiates an I2C communication as master receiver, and receives one byte from the device: ACK or NACK or BUSY.
- Receive Data frame: The host initiates an I2C communication as master receiver, and receives the response from the device. The number of received bytes depends on the command.
- Send Data frame: The host initiates an I2C communication as master transmitter, and sends the needed bytes to the device. The number of transmitted bytes depends on the command.

Caution: For Write, Erase and Read Unprotect commands, the host must respect the related timings (i.e. page write, sector erase), as specified in product datasheets. As an example, when launching an Erase command, the host has to wait (before the last ACK of the command) for a duration equivalent to the maximum sector/page erase time specified in datasheet (or at least the typical sector/page erase time).
**Caution:** For I2C communication, a timeout mechanism is implemented, it must be respected for bootloader commands to be executed correctly. This timeout is implemented between two I2C frames in the same command. For example, for a Write memory command, a timeout is inserted between the command-sending frame and address memory-sending frame. Also, the same timeout period is inserted between two successive instances of data reception or transmission in the same I2C frame. If the timeout period has elapsed, a system reset is generated to avoid a bootloader crash. Refer to the section dedicated to I2C connection timing of AN2606 to get the I2C timeout value for each STM32 product.

### 2.1 Get command

The Get command allows the user to get the version of the bootloader and the supported commands. When the bootloader receives the Get command, it transmits the bootloader version and the supported command codes to the host, as described in Figure 2.

**Figure 2. Get command: host side**

```
Start Get

Send Command frame (0x00 + 0xFF)

Wait for ACK or NACK frame

NACK

ACK

Receive data frame:
- number of bytes
- bootloader version
- list of supported commands

Wait for ACK or NACK frame

NACK

ACK

End of Get
```
Figure 3. Get command: device side

Start Get

Received frame = 0x00+0xFF?

Yes

Send ACK frame

Send data frame:
- number of bytes to be sent
- bootloader version
- list of supported commands

Send ACK frame

End of Get

No

Send NACK frame
The STM32 sends the bytes as follows:

- **For I2C protocol V1.0:**
  - Byte 1: ACK
  - Byte 2: N = 11 = the number of bytes to follow - 1 except current and ACKs
  - Byte 3: Bootloader version 0x10 = Version 1.0
  - Byte 4: 0x00 - Get command
  - Byte 5: 0x01 - Get Version
  - Byte 6: 0x02 - Get ID
  - Byte 7: 0x11 - Read Memory command
  - Byte 8: 0x21 - Go command
  - Byte 9: 0x31 - Write Memory command
  - Byte 10: 0x44 - Erase command
  - Byte 11: 0x63 - Write Protect command
  - Byte 12: 0x73 - Write Unprotect command
  - Byte 13: 0x82 - Readout Protect command
  - Byte 14: 0x92 - Readout Unprotect command
  - Byte 15: ACK

- **For I2C protocol V1.1:**
  - Byte 1: ACK
  - Byte 2: N = 17 = the number of bytes to follow - 1 except current and ACKs
  - Byte 3: Bootloader version 0x11 = Version 1.1
  - Byte 4: 0x00 - Get command
  - Byte 5: 0x01 - Get Version
  - Byte 6: 0x02 - Get ID
  - Byte 7: 0x11 - Read Memory command
  - Byte 8: 0x21 - Go command
  - Byte 9: 0x31 - Write Memory command
  - Byte 10: 0x44 - Erase command
  - Byte 11: 0x63 - Write Protect command
  - Byte 12: 0x73 - Write Unprotect command
  - Byte 13: 0x82 - Readout Protect command
  - Byte 14: 0x92 - Readout Unprotect command
  - Byte 15: 0x32 - No-Stretch Write Memory command
  - Byte 16: 0x45 - No-Stretch Erase command
  - Byte 17: 0x64 - No-Stretch Write Protect command
  - Byte 18: 0x74 - No-Stretch Write Unprotect command
  - Byte 19: 0x83 - No-Stretch Readout Protect command
  - Byte 20: 0x93 - No-Stretch Readout Unprotect command
  - Byte 21: ACK
2.2 Get Version command

The Get Version command is used to get the I2C bootloader version. When the bootloader receives the command, it transmits the information described below (bootloader version) to the host.

The STM32 sends the bytes as follows:

- Byte 1: ACK
- Byte 2: Bootloader version (0 < Version ≤255) (for example, 0x10 = Version 1.0)
- Byte 3: ACK
### 2.3 Get ID command

The Get ID command is used to get the version of the chip ID (identification). When the bootloader receives the command, it transmits the product ID to the host.

The STM32 device sends the bytes as follows:
- Byte 1: ACK
- Byte 2: \( N = \text{the number of bytes} - 1 \) (for STM32, \( N = 1 \)), except for current byte and ACKs
- Bytes 3-4: PID (product ID)
  - Byte 3 = MSB
  - Byte 4 = LSB
- Byte 5: ACK
1. GID = Get ID.

Figure 6. Get ID command: host side

- Start GID(1)
- Send command frame (0x02+0xFD)
- Wait for ACK or NACK frame
- Receive data frame:
  - number of bytes - 1
  - product ID
- Wait for ACK or NACK frame
- End of GID(1)

Figure 7. Get ID command: device side

- Start GID(1)
- Received frame = 0x02+0xFD?
- Send NACK frame
- Send ACK frame
- Send data frame:
  - number of bytes - 1
  - product ID
- Send ACK frame
- End of GID(1)

1. GID = Get ID.
2.4 Read Memory command

The Read Memory command is used to read data from any valid memory address.

When the bootloader receives the Read Memory command, it transmits the ACK byte to the application. The bootloader then waits for a 4-byte address (byte 1 is the address MSB, byte 4 is the LSB) and a checksum byte, then it checks the received address. If the address is valid and the checksum is correct, the bootloader transmits an ACK byte; otherwise, it transmits a NACK byte and aborts the command.

If the address is valid and the checksum is correct, the bootloader waits for the number of bytes to be transmitted (N bytes), and for its complemented byte (checksum). If the checksum is correct, the bootloader transmits the needed data to the application, starting from the received address. If the checksum is not correct, it sends a NACK before aborting the command.

The host sends bytes to the STM32 as follows:
1. Bytes 1-2: 0x11 + 0xEE
2. Wait for ACK
3. Bytes 3-6: Start address (byte 3: MSB, byte 6: LSB)
4. Byte 7: Checksum: XOR (byte 3, byte 4, byte 5, byte 6)
5. Wait for ACK
6. Byte 8: The number of bytes to be read - 1 (0 < N ≤ 255)
7. Byte 9: Checksum: XOR byte 8 (complement of byte 8)
Figure 8. Read Memory command: host side

1. RM = Read Memory.
Figure 9. Read Memory command: device side

1. RM = Read Memory.
2.5 Go command

The Go command is used to execute the downloaded code or any other code, by branching to an address specified by the application. When the bootloader receives the Go command, it transmits the ACK byte to the application. The bootloader then waits for a 4-byte address (byte 1 is the address MSB, byte 4 is the LSB) and a checksum byte, then checks the received address. If the address is valid and the checksum is correct, the bootloader transmits an ACK byte; otherwise, it transmits a NACK byte and aborts the command.

When the address is valid and the checksum is correct, the bootloader firmware performs the following operations:

1. Initializes the registers of the peripherals used by the bootloader to their default reset values
2. Initializes the user application main stack pointer
3. Jumps to the memory location programmed in the received ‘address + 4’ (corresponds to the address of the application reset handler). For example, if the received address is 0x08000000, the bootloader jumps to the memory location programmed at address 0x08000004.

In general, the host sends the base address where the application to jump to is programmed.

Note: Jumping to the application only works if the user application correctly sets the vector table to point to the application address.

The host sends bytes to the STM32 as follows:

1. Byte 1: 0x21
2. Byte 2: 0xDE
3. Wait for ACK
4. Byte 3 to byte 6: start address
   - Byte 3: MSB
   - Byte 6: LSB
5. Byte 7: checksum: XOR (byte 3, byte 4, byte 5, byte 6)
6. Wait for ACK
Figure 10. Go command: host side

Start GO

Send command frame (0x21 + 0xDE)

Wait for ACK or NACK frame

ACK

Send data frame: Start Address (4 bytes) and checksum

Wait for ACK or NACK frame

ACK

NACK

End of GO

NACK
Figure 11. Go command: device side

1. Start GO
2. Received frame = 0x21+0xDE?
   - Yes: ROP active?
     - Yes: Send ACK frame
       - Receive data frame: start address (4 bytes) and checksum
         - Address valid & checksum OK?
           - Yes: Send ACK frame
             - Jump to user application
           - No: Send NACK frame
             - End of GO
         - No: Jump to user application
   - No: Send ACK frame

Note: ROP active means Read Operation Permission.
2.6 Write Memory command

The Write Memory command is used to write data to any valid memory address (see Note: below) of RAM, Flash memory, or the option byte area.

When the bootloader receives the Write Memory command, it transmits the ACK byte to the application. The bootloader then waits for a 4-byte address (byte 1 is the address MSB, and byte 4 is the LSB) and a checksum byte, and then checks the received address.

If the received address is valid and the checksum is correct, the bootloader transmits an ACK byte; otherwise, it transmits a NACK byte and aborts the command. When the address is valid and the checksum is correct, the bootloader:

1. gets a byte, N, which contains the number of data bytes to be received
2. receives the user data ((N + 1) bytes) and the checksum (XOR of N and of all data bytes)
3. programs the user data to memory, starting from the received address.

At the end of the command, if the write operation is successful, the bootloader transmits the ACK byte; otherwise, it transmits a NACK byte to the application and aborts the command.

If the Write Memory command is issued to the option byte area, all options are erased before writing the new values. At the end of the command, the bootloader generates a system reset to take the new configuration of the option byte into account.

The maximum length of the block to be written to the option bytes depends upon the STM32 product, and the address received from the host must be the start address of the option byte area. For more information about option bytes, refer to the STM32 product reference manual.

Note: The maximum length of the block to be written to RAM or Flash memory is 256 bytes.

When writing to the RAM, take care not to overlap the first RAM used by the bootloader firmware.

No error is returned when performing write operations to write-protected sectors.

The host sends the bytes to the STM32 as follows:

1. Byte 1: 0x31
2. Byte 2: 0xCE
3. Wait for ACK
4. Byte 3 to byte 6: Start address
   - Byte 3: MSB
   - Byte 6: LSB
5. Byte 7: Checksum: XOR (byte 3, byte 4, byte 5, byte 6)
6. Wait for ACK
7. Byte 8: Number of bytes to be received (0 < N ≤ 255)
8. N + 1 data bytes: (max 256 bytes)
9. Checksum byte: XOR (N, N+1 data bytes)
10. Wait for ACK
Figure 12. Write Memory command: host side

1. WM = Write Memory.
Figure 13. Write Memory command: device side

1. WM = Write Memory.
2.7 Erase Memory command

The Erase Memory command allows the host to erase Flash memory pages or sectors using a two-byte addressing mode. When the bootloader receives the Erase Memory command, it transmits the ACK byte to the host. The bootloader then receives two bytes (number of pages or sectors to be erased), the Flash memory page or sector codes (each of which is coded on two bytes, MSB first) and a checksum byte (XOR of the sent bytes). If the checksum is correct, the bootloader erases the memory and sends an ACK byte to the host; otherwise, it sends a NACK byte to the host and the command is aborted.

Erase Memory command specifications

The bootloader receives one half-word (two bytes) that contains the number of pages or sectors to be erased diminished by 1. If 0xFFFY is received (where Y is from 0 to F), a special erase is performed (0xFFFF for global mass erase, 0xFFFE and 0xFFFD, respectively, for bank1 and bank2 mass erase).

The bootloader receives:
- in the case of a special erase, one byte: the checksum of the previous bytes (e.g. 0x00 for 0xFFFF)
- in the case of a N pages or sectors are erased, the bootloader receives 2 x N bytes, each half-word of which contains a page or sector number that is coded on two bytes, with the MSB first. Then all previous byte checksums are received in one byte.

Note: Some products do not support the mass erase feature, in this case use the erase command to erase all pages or sectors. The maximum number of pages or sectors is product-related, and must be respected. The maximum number of pages or sectors that can be erased in the same command is 512. Codes from 0xFFFC to 0xFFF0 are reserved.

No error is returned when performing erase operations on write-protected sectors.

The host sends bytes to the STM32 as follows:
1. Byte 1: 0x44
2. Byte 2: 0xBB
3. Wait for ACK

- For Special erase:
4. Bytes 3-4: Special erase (0xFFFx)
5. Bytes 5: Checksum of Bytes 3-4
6. Wait for ACK

- For Page erase:
7. Bytes 3-4: Number of pages or sectors to be erased - 1
8. Bytes 5: Checksum of Bytes 3-4
9. Wait for ACK
10. (2 x N) bytes (page numbers or sectors coded on two bytes MSB first) and then the checksum for these bytes.
11. Wait for ACK

- Example of I2C frame:
  - erase page 1:
0x44 0xBB **Wait ACK** 0x00 0x00 0x00 **Wait ACK** 0x00 0x01 0x01 **Wait ACK**

- erase page 1 and page 2:

0x44 0xBB **Wait ACK** 0x00 0x01 0x01 **Wait ACK** 0x00 0x01 0x00 0x00 0x02 0x03 **Wait ACK**

**Figure 14. Erase Memory command: host side**

1. ER = Erase Memory.

**Note:** Some products do not support the Special erase feature. For these products, this command is NACK-ed.
Figure 15. Erase Memory command: device side

1. ER = Erase Memory.
2. Requested Special erase command is NACK-ed if not supported by the used STM32 product.
2.8 Write Protect command

The Write Protect command is used to enable the write protection for some or all Flash memory sectors. When the bootloader receives the Write Protect command, it transmits the ACK byte to the host. The bootloader then waits for the number of bytes to be received (sectors to be protected), and then receives the Flash memory sector codes from the application.

At the end of the Write Protect command, the bootloader transmits the ACK byte and generates a system reset to take the new configuration of the option byte into account.

The Write Protect command sequence is as follows:

- The bootloader receives one byte that contains N, the number of sectors to be write-protected - 1 (0 ≤ N ≤ 255).
- The bootloader receives (N + 1) bytes, each of them containing a sector code.

Note: Neither the total number of sectors, nor the number of the sector to be protected are checked. This means that no error is returned when a command is passed with either a wrong number of sectors to be protected, or with a wrong sector number.

If a second Write Protect command is executed, the Flash memory sectors protected by the first command become unprotected, and only the sectors passed with the second Write Protect command become protected.
Figure 16. Write Protect command: host side

1. WP = Write Protect.
Figure 17. Write Protect command: device side

1. WP = Write Protect.
2.9 Write Unprotect command

The Write Unprotect command is used to disable the write protection of all Flash memory sectors. When the bootloader receives the Write Unprotect command, it transmits the ACK byte to the host. The bootloader then disables the write protection of all Flash memory sectors, and transmits the ACK byte.

A system reset is generated to take the new configuration of the option byte into account.

Figure 18. Write Unprotect command: host side

1. WPUN = Write Unprotect.
2.10 Readout Protect command

The Readout Protect command is used to enable the Flash memory read protection. When the bootloader receives the Readout Protect command, it transmits the ACK byte to the host, and enables the read protection for the Flash memory.

At the end of the Readout Protect command, the bootloader transmits the ACK byte and generates a system reset to take the new configuration of the option byte into account.
Figure 20. Readout Protect command: host side

1. RDP_PRM = Readout Protect.

Figure 21. Readout Protect command: device side

1. RDP_PRM = Readout Protect.
2.11 Readout Unprotect command

The Readout Unprotect command is used to disable Flash memory read protection. When the bootloader receives the Readout Unprotect command, it transmits the ACK byte to the host.

The bootloader then disables the read protection for the entire Flash memory, which results in an erasure of the entire Flash memory. If the operation is unsuccessful, the bootloader transmits a NACK, and the read protection remains active.

Note: This operation takes the same time to erase all pages or sectors (or to perform a mass erase if it is supported by the product), so the host has to wait until the end of the operation. For the Flash memory erase timings refer to the product datasheet.

At the end of the Readout Unprotect command, the bootloader transmits an ACK and generates a system reset to take the new configuration of the option byte into account.

Figure 22. Readout Unprotect command: host side

1. RDU_PRM = Readout Unprotect.
Figure 23. Readout Unprotect command: device side

1. RDU_PRM = Readout Unprotect.
2.12 No-Stretch Write Memory command

The No-Stretch Write Memory command is used to write data to any valid memory area.

When the bootloader receives the No-Stretch Write Memory command, it transmits the ACK byte to the application. The bootloader then waits for a 4-byte address (byte 1 is the address MSB, and byte 4 is the LSB) and a checksum byte, and then checks the received address.

If the received address is valid and the checksum is correct, the bootloader transmits an ACK byte; otherwise, it transmits a NACK byte and aborts the command. When the address is valid and the checksum is correct, the bootloader:

1. Gets a byte, N, which contains the number of data bytes to be received
2. Receives the user data ((N + 1) bytes) and the checksum (XOR of N and of all data bytes)
3. Programs the user data to memory, starting from the received address
4. Returns a Busy state (0x76) while operation is ongoing

At the end of the command, if the write operation is successful, the bootloader transmits the ACK byte; otherwise, it transmits a NACK byte to the application and aborts the command.

Note: If the No-Stretch Write Memory command is issued to the option byte area, the bootloader generates a system reset to take the new configuration of the option byte into account.

The maximum length of the block to be written to memory is 256 bytes except for the option bytes the maximum length depends on the STM32 product, and the address received from the host must be the start address of the option byte area. For more information, refer to the STM32 product reference manual.

No error is returned when performing write operations to write-protected sectors.

The host sends the bytes to the STM32 as follows:

1. Byte 1: 0x32
2. Byte 2: 0xCD
3. Wait for ACK
4. Byte 3 to byte 6: Start address
   - Byte 3: MSB
   - Byte 6: LSB
5. Byte 7: Checksum: XOR (byte 3, byte 4, byte 5, byte 6)
6. Wait for ACK
7. Byte 8: Number of bytes to be received (0 < N ≤ 255)
8. N +1 data bytes: (Max 256 bytes)
9. Checksum byte: XOR (N, N+1 data bytes)
10. Wait for ACK (if Busy keep polling on ACK/NACK)
Figure 24. No-Stretch Write Memory command: host side

1. WM = Write Memory.
Figure 25. No-Stretch Write Memory command: device side

1. WM = Write Memory.
2.13 No-Stretch Erase Memory command

The No-Stretch Erase Memory command allows the host to erase Flash memory pages or sectors using a two-byte addressing mode. When the bootloader receives the Erase Memory command, it transmits the ACK byte to the host. The bootloader then receives two bytes (number of pages or sectors to be erased), the Flash memory page or sector codes (each of which is coded on two bytes, MSB first) and a checksum byte (XOR of the sent bytes). If the checksum is correct, the bootloader erases the memory (returns Busy state (0x76) while operation is ongoing) then sends an ACK byte to the host; otherwise, it sends a NACK byte to the host and the command is aborted.

No-Stretch Erase Memory command specifications

The bootloader receives one half-word (two bytes) that contains the number of pages or sectors to be erased diminished by 1. If 0xFFFY is received (where Y is from 0 to F), a special erase is performed (0xFFFF for global mass erase, 0xFFFE and 0xFFFFD respectively for bank1 and bank2 mass erase).

The bootloader receives:
- In the case of a special erase, one byte: the checksum of the previous bytes (e.g. 0x00 for 0xFFFF)
- In the case of a N pages or sectors are erased, the bootloader receives (2 x N ) bytes, each half-word of which contains a page or sector number that is coded on two bytes, with the MSB first. Then all previous byte checksums are received in one byte.

Note: Some products do not support the mass erase feature, in this case use the erase command to erase all pages or sectors instead.
The maximum number of pages or sectors is relative to the product, and must be respected. The maximum number of pages or sectors that can be erased in the same command is 512. Codes from 0xFFF to 0xFFFF0 are reserved.
No error is returned when performing erase operations on write-protected sectors.

The host sends bytes to the STM32 as follows:
1. Byte 1: 0x45
2. Byte 2: 0xBA
3. Wait for ACK
   - For Special erase:
4. Bytes 3-4: Special erase (0xFFFx)
5. Bytes 5: Checksum of bytes 3-4
6. Wait for ACK (if Busy keep polling on ACK/NACK)
   - For Page erase:
7. Bytes 3-4: Number of pages or sectors to be erased - 1
8. Bytes 5: Checksum of bytes 3-4
9. Wait for ACK
10. (2 x N) bytes (page numbers or sectors coded on two bytes MSB first) and then the checksum for these bytes.
11. Wait for ACK (if Busy keep polling on ACK/NACK)
   - Example of I2C frame:
     – erase page 1:
0x45 0xBA  **Wait ACK**  0x00 0x00 0x00 0x00  **Wait ACK**  0x00 0x01 0x01  **Wait ACK**

- erase page 1 and page 2:

0x45 0xBA  **Wait ACK**  0x00 0x01 0x01  **Wait ACK**  0x00 0x01 0x00 0x02 0x03  **Wait ACK**

**Figure 26. No-Stretch Erase Memory command: host side**

1. ER = Erase Memory.

*Note:* Some products do not support the Special erase feature. For these products, this command is NACK-ed.
Figure 27. No-Stretch Erase Memory command: device side

1. ER = Erase Memory.
2. Requested Special erase command is NACK-ed if not supported by the used STM32 product.
2.14 **No-Stretch Write Protect command**

The No-Stretch Write Protect command is used to enable the write protection for some or all Flash memory sectors. When the bootloader receives the Write Protect command, it transmits the ACK byte to the host. The bootloader then waits for the number of bytes to be received (sectors to be protected), then receives the Flash memory sector codes from the application and returns Busy state (0x76) while operation is ongoing.

At the end of the No-Stretch Write Protect command, the bootloader transmits the ACK byte and generates a system reset to take the new configuration of the option byte into account.

The Write Protect command sequence is as follows:

- The bootloader receives one byte that contains $N$, the number of sectors to be write-protected - 1 ($0 \leq N \leq 255$).
- The bootloader receives $(N + 1)$ bytes, each byte of which contains a sector code.

**Note:** Neither the total number of sectors, nor the sector number to be protected are checked. This means that no error is returned when a command is passed with either a wrong number of sectors to be protected, or a wrong sector number.

If a second Write Protect command is executed, the Flash memory sectors that had been protected by the first command become unprotected, and only the sectors passed within the second Write Protect command become protected.
Figure 28. No-Stretch Write Protect command: host side

1. WP = Write Protect.
1. WP = Write Protect.
2.15 No-Stretch Write Unprotect command

The No-Stretch Write Unprotect command is used to disable the write protection of all Flash memory sectors. When the bootloader receives the Write Unprotect command, it transmits the ACK byte to the host. The bootloader then disables the write protection of all Flash memory sectors, returns Busy state (0x76) while operation is ongoing. At the end it transmits the ACK byte.

A system reset is generated to take the new configuration of the option byte into account.

Figure 30. No-Stretch Write Unprotect command: host side

1. WPUN = Write Unprotect.
1. WPUN = Write Unprotect.
2.16 No-Stretch Readout Protect command

The No-Stretch Readout Protect command is used to enable the Flash memory read protection. When the bootloader receives the Readout Protect command, it transmits the ACK byte to the host, enables the read protection for the Flash memory and returns Busy state (0x76) while operation is ongoing.

At the end of the No-Stretch Readout Protect command, the bootloader transmits the ACK byte and generates a system reset to take the new configuration of the option byte into account.

Figure 32. No-Stretch Readout Protect command: host side

1. RDP_PRM = Readout Protect.
Figure 33. No-Stretch Readout Protect command: device side

1. RDP_PRM = Readout Protect.
2.17 No-Stretch Readout Unprotect command

The No-Stretch Readout Unprotect command is used to disable Flash memory read protection. When the bootloader receives the Readout Unprotect command, it transmits the ACK byte to the host.

The bootloader then disables the read protection for the entire Flash memory, which results in an erasure of the entire Flash memory and returns Busy state (0x76) while operation is ongoing. If the operation is unsuccessful, the bootloader transmits a NACK, and the read protection remains active.

At the end of the No-Stretch Readout Unprotect command, the bootloader transmits an ACK and generates a system reset to take the new configuration of the option byte into account.

Figure 34. No-Stretch Readout Unprotect command: host side

1. RDU_PRM = Readout Unprotect.
Figure 35. No-Stretch Readout Unprotect command: device side

1. RDU_PRM = Readout Unprotect.
3 Bootloader protocol version evolution

Table 3 lists the bootloader versions.

<table>
<thead>
<tr>
<th>Version</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.0</td>
<td>Initial protocol version.</td>
</tr>
<tr>
<td>V1.1</td>
<td>This version implements new I2C commands: No-Stretch Write Memory, No-Stretch Erase Memory, No-Stretch Write Protect, No-Stretch Write Unprotect, No-Stretch ReadOut Protect and No-Stretch ReadOut Unprotect.</td>
</tr>
</tbody>
</table>
# Revision history

### Table 4. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>18-Jan-2013</td>
<td>1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
| 02-May-2014   | 2        | Updated list of Applicable products in Table 1.  
|               |          | Updated set of commands in Table 2. |
|               |          | Updated Section 2: Bootloader command set.  
|               |          | Added Section 2.12, Section 2.13, Section 2.14, Section 2.15,  
|               |          | Section 2.16 and Section 2.17.  
|               |          | Added new Protocol version in Table 3. |
| 08-Oct-2015   | 3        | Updated Introduction, Section 2: Bootloader command set, Section 2.7:  
|               |          | Erase Memory command and Section 2.13: No-Stretch Erase Memory command.  
|               |          | Updated Table 1: Applicable products and Table 2: I2C bootloader commands.  
|               |          | Updated Figure 14: Erase Memory command: host side, Figure 15:  
|               |          | Erase Memory command: device side, Figure 26: No-Stretch Erase Memory command: host side and Figure 27: No-Stretch Erase Memory command: device side. |
| 19-Oct-2016   | 4        | Updated Introduction and Table 1: Applicable products. |
| 15-Mar-2017   | 5        | Updated Table 1: Applicable products. |
| 15-Jan-2019   | 6        | Updated Table 1: Applicable products.  
|               |          | Updated Section 1: I2C bootloader code sequence.  
|               |          | Minor text edits across the whole document. |
| 05-Apr-2019   | 7        | Updated Table 1: Applicable products. |
| 23-Sep-2019   | 8        | Updated Table 1: Applicable products. |