Migrating from STM32L0, STM32L1, and STM32L4 Series associated with SX12xx transceivers to STM32WL Series microcontrollers

Introduction

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may force the user to switch to smaller components and to shrink the PCB area.

This application note details the steps needed to migrate:

- from an existing application based on a microcontroller of the STM32L0, STM32L1 or STM32L4 Series, associated with one SX12xx Semtech LoRa® transceiver
- to an application based on a microcontroller of the STM32WL Series

This document lists the main features that are necessary to build a LoRaWAN® application on STM32L0, STM32L1 or STM32L4 Series and the equivalent features of STM32WL Series devices. For more details, see the reference manuals and datasheets of the products.

A good knowledge of SX12xx Semtech transceivers is also needed.

Table 1. Applicable products

Reference	Products
STM32L0/1/4	STM32L0 Series, STM32L1 Series, STM32L4 Series
STM32WL	STM32WL Series

1 System overview

Several hardware models target sub-GHz RF communications. This document focus on the ones supported by LoRaWAN STM32Cube firmwares for STM32L1/2/4 and STM32WL Arm® Cortex®-M based microcontrollers.

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1.1 STM32L0/L1/L4 devices + SX12xx radio

1.1.1 I-CUBE-LRWAN Expansion Package

The firmware package supporting LoRaWAN is the I-CUBE-LRWAN Expansion Package. Refer to the user manual *STM32 LoRa® Expansion Package for STM32Cube* (UM2073) for more details.

I-CUBE-LRWAN implements LoRaWAN on low-power STM32L0/1/4 microcontrollers, driving external radios.

The following examples are embedded in the package:

- **End_Node**: autonomous software integrating the application layer, the MAC Layer and the PHY driver (all implemented on the MCU)
- **AT_Slave**: modem specifically designed for the CMWX1ZZABZ long-range Murata module
- **PingPong**: simple Rx/Tx RF link between two devices that exercise only physical layer (no MAC layer)

The configurations detailed in the next sections are supported by I-CUBE-LRWAN.

1.1.2 Two-chips application

The STM32L0/1/4 MCU drives an **external** SX12xx Semtech radio. In I-CUBE-LRWAN, a LoRa end-device is built by stacking a Semtech radio expansion board onto an STM32 Nucleo board.

The table below presents the supported configurations.

Table 2. I-CUBE-LRWAN supported hardware

Semtech/ST boards	NUCLEO-L053R8	NUCLEO-L073RZ	NUCLEO-L152RE	NUCLEO-L476RG
SX1276MB1MAS	X(1)	X	X	X
SX1276MB1LAS	X	X	X	X
SX1272MB2DAS	X	X	X	X
SX1261DVK1BAS	X	X	X	X
SX1262DVK1CAS	X	X	X	X
SX1262DVK1DAS	X	X	X	X

1. *X = supported.*

The two Semtech radio generations featuring LoRa modulation are described in the next sections.

1.1.2.1 *SX127x radios*

Introduced first, these radios feature LoRa, (G)FSK/(G)MSK, and OOK modulations and can work on both high band and low band. SX1272 is a lower-cost version, high-band only transceiver. SX1278 is the low-band counterpart.

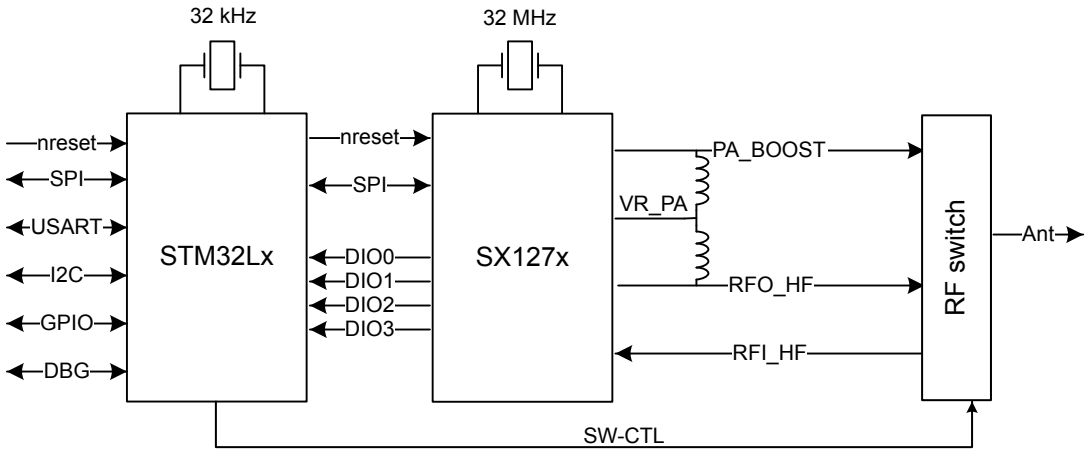
The table below lists the characteristics of several expansion boards available.

Table 3. Semtech radio shield characteristics

Board	Characteristics
SX1276MB1MAS	868 MHz (HF) at 14 dBm and 433 MHz (LF) at 14 dBm
SX1276MB1LAS	915 MHz (HF) at 20 dBm and 433 MHz (LF) at 14 dBm
SX1272MB2DAS	915 MHz and 868 MHz at 14 dBm
SX1261DVK1BAS	E406V03A SX1261, 14 dBm, 868 MHz, XTAL
SX1262DVK1CAS	E428V03A SX1262, 22 dBm, 915 MHz, XTAL
SX1262DVK1DAS	E449V01A SX1262, 22 dBm, 860-930 MHz, TCXO

The figure below shows the main interconnections between the MCU and the SX127xx.

Figure 1. General principle of STM32Lx/SX127x connections



Few STM32 peripherals are reserved to drive the SX127x radio:

- **Reset**: One MCU GPIO is used to reset the radio. A reset of the radio is performed at radio start-up.
- **SPI**: The SX1276 radio registers are accessed through the SPI bus at 8 Mbit/s. SPI NSS is a GPIO controlled by software during SPI accesses.
- **RF switch**: depending on board types, from one to three GPIOs are required to drive the RF switch in different state (for example: Off, Rx or Tx).
- **DIOx**: up to six GPIOs must be configured in interrupt input to receive events from the radio. For more details, refer to the user manual *STM32 LoRa® Expansion Package for STM32Cube* (UM2073).
  - DIO0 is used to signal a rxDone or txDone event to the MCU.
  - DIO1 is used to signal a RxTimeout or TxTimeout event to the MCU.
  - DIO2 is used to signal that a FSK synchronization is found.
  - DIO3 is used to signal that a clear activity detection is done.

1.1.2.2 *SX126x radios*

The new Semtech RF transceiver are the SX1261 and SX1262, about four times smaller than SX127x and able to transmit/receive signals from 150 MHz up to 960 MHz.

The SX126x radio access differs from the SX127x radio access in several ways:

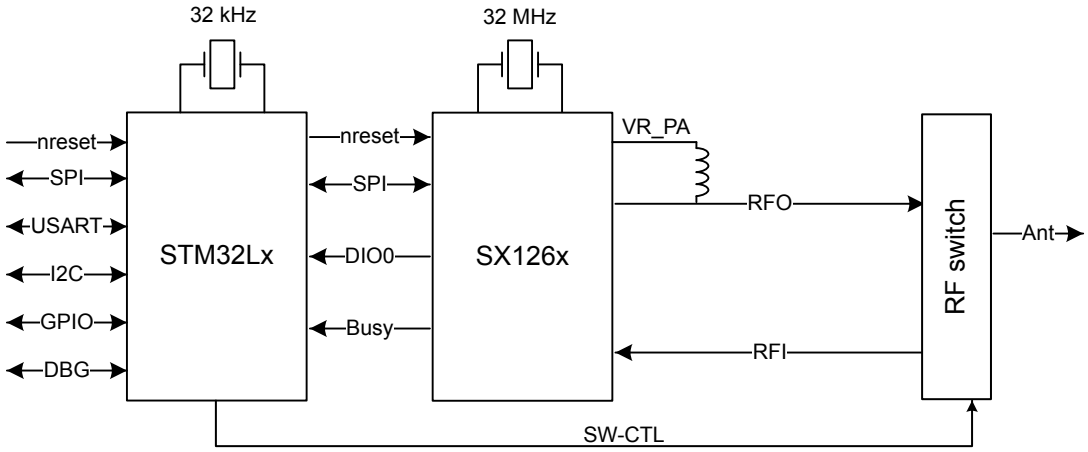
- SX126x implements a command interface over SPI, while on SX127x, SPI allows register access only.
- The Busy signal informs the MCU that a radio command is being processed. The MCU must then monitor the Busy signal before sending new commands.
- Only DIO0 is sufficient to report any event to the STM32.
- MCU GPIOs must be reserved depending on the RF switch control requirements.

The only difference between SX1261 and SX1262 is the output power capability:

- SX1261 is limited to 14 dBm and is optimized for this output power. Its output power pin is RFO_LP.
- SX1262 is limited to 22 dBm and is optimized for this output power. Its output power pin is RFO_HP (note that, to generate a 14 dBm wave, the SX1262 consumes 50 % more current than a SX1261 for the same output power).

The figure below shows the main interconnections between the STM32Lx and the SX126x.

Figure 2. General principle of STM32Lx/SX126x connections



Few STM32 peripherals are reserved to drive the SX126x:

- Reset: One MCU GPIO is used to reset the radio. A reset of the radio is performed at radio startup.
- SPI: The SX1276 radio registers are accessed through the SPI bus at 8 Mbit/s. Radio NSS is a GPIO controlled by software during SPI accesses.
- RF switch: depending on board types, from one to three GPIOs are required to drive the RF switch in different state (for example: Off, Rx, Tx high power, or Tx low power).
- DIO0: signals an event to the MCU (rxDone, txDone, RTxtimout, CAD done)
- Busy: one GPIO is configured in input mode (only for SX126x).

1.1.3 Two chips in one module

In order to ease customer experiences, the CMWX1ZZABZ long-range Murata module is based on one STM32L072 MCU plus one SX1276 Semtech radio. This module features a 32,768 kHz RTC clock and a 32 MHz TCXO. RF matching components are also embedded in the module. The matching network is optimized from 864 to 930 MHz, ensuring high-band worldwide compatibility.

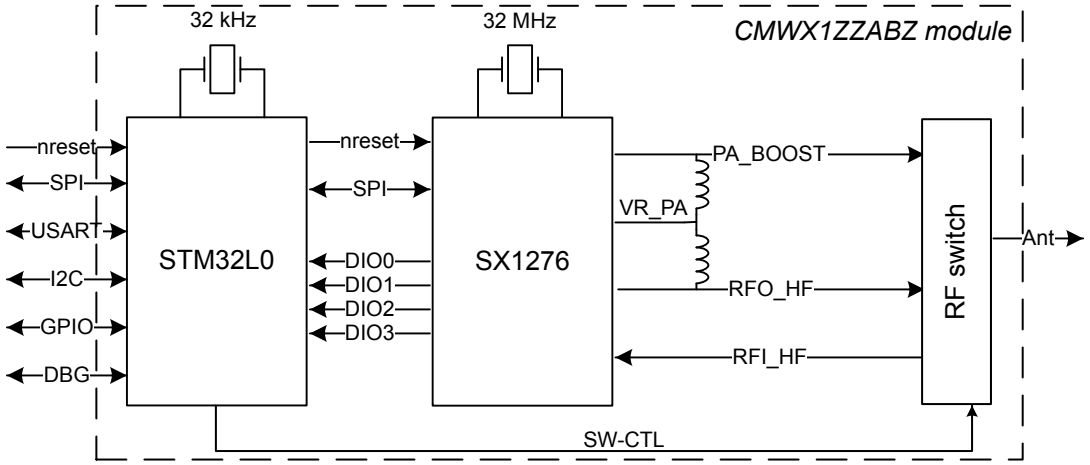
The main advantages of the CMWX1ZZABZ module are listed below:

- Optimized and guaranteed RF matching (matching network requires specific RF knowledge and expensive RF equipment)
- Modular Regulatory certification (FCC/ETSI, ARIB) done by the module maker, can be inherited by the user to pass a reduced set of tests
- Stack certification that can also be inherited if the firmware on the module remains unchanged

On the CMWX1ZZABZ module, the following RF pins are connected to the RF switch pads:

- RF RX
- RFO_HF (RF low power) for the 14 dBm regions
- PABOOST (RF high power) for the 20 dBm regions

Figure 3. CMWX1ZZABZ module overview



1.2 STM32WL devices

The main difference versus the STM32L0/1/4 devices is that STM32WL devices embed a built-in radio peripheral, named sub-GHz radio system. No more need of external RF transceivers.

BUSY and DIO0 lines are internally connected to bits of the PWR registers. A dedicated internal SPI peripheral is integrated to communicate with the sub-GHz radio.

Note: The STM32WL devices can reuse the clock provided by the radio XTAL or TCXO as HSE, that is fixed at 32 MHz.

The LDO/SMPS block of the sub-GHz radio is reused for the rest of the subsystem. Refer to the product datasheet and reference manuals for more details on the sub-GHz radio integration in STM32WL devices.

Figure 4. Sub-GHz radio peripheral in STM32WLEx devices

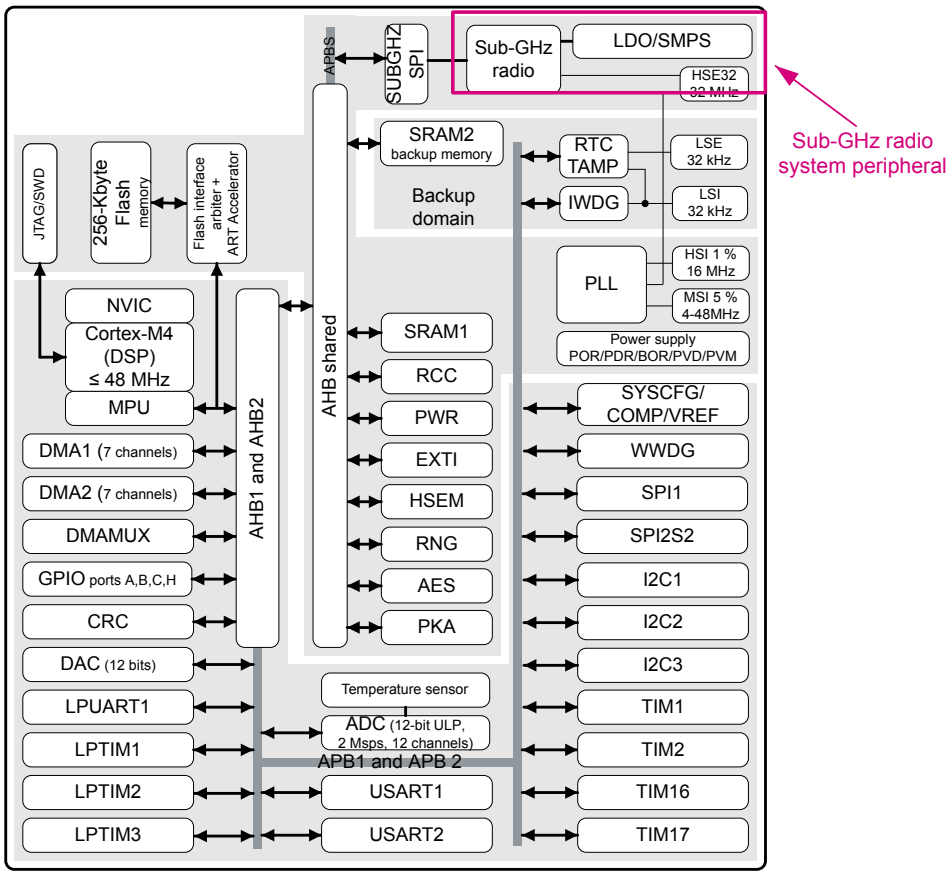
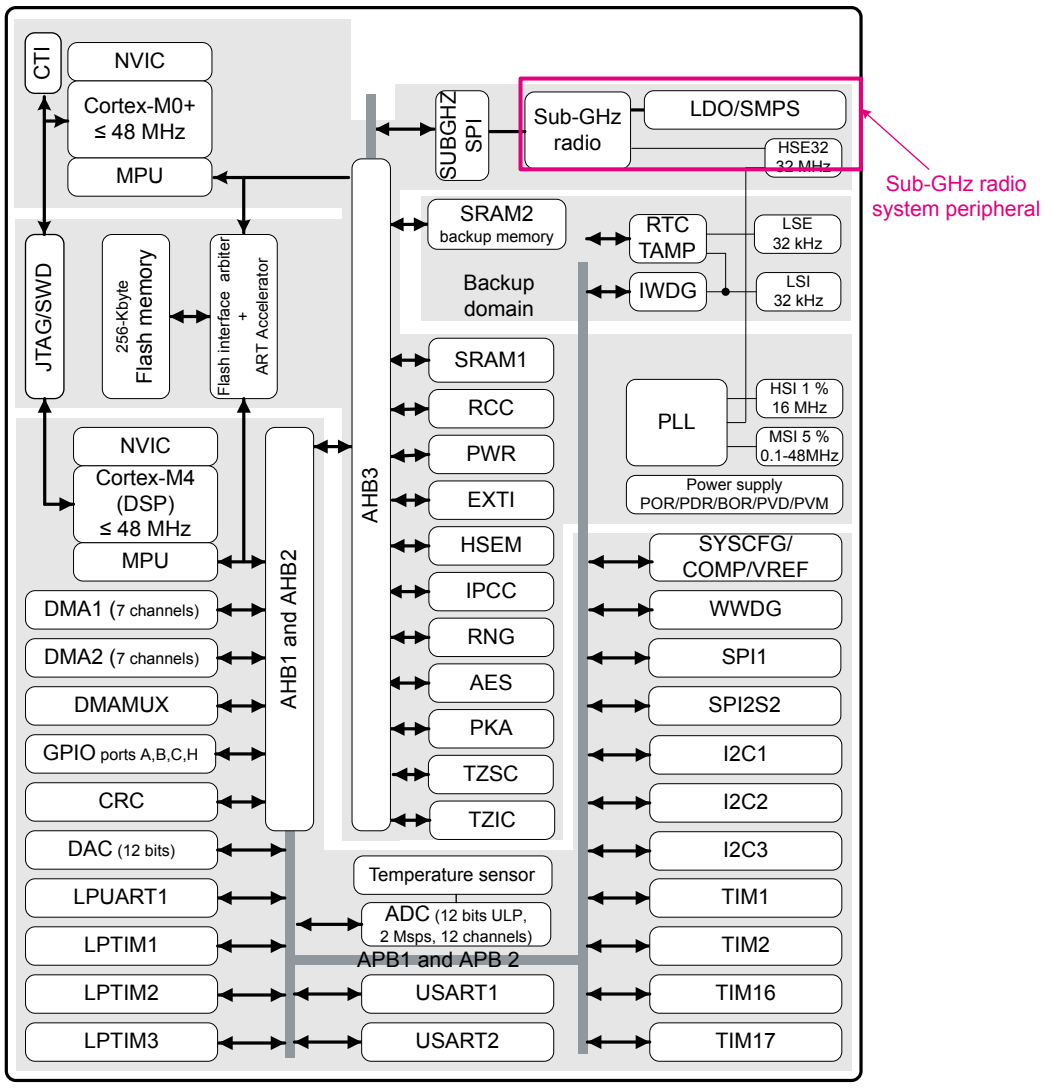


Figure 5. **Sub-GHz radio peripheral in STM32WL5x devices**



1.2.1 Supply strategy

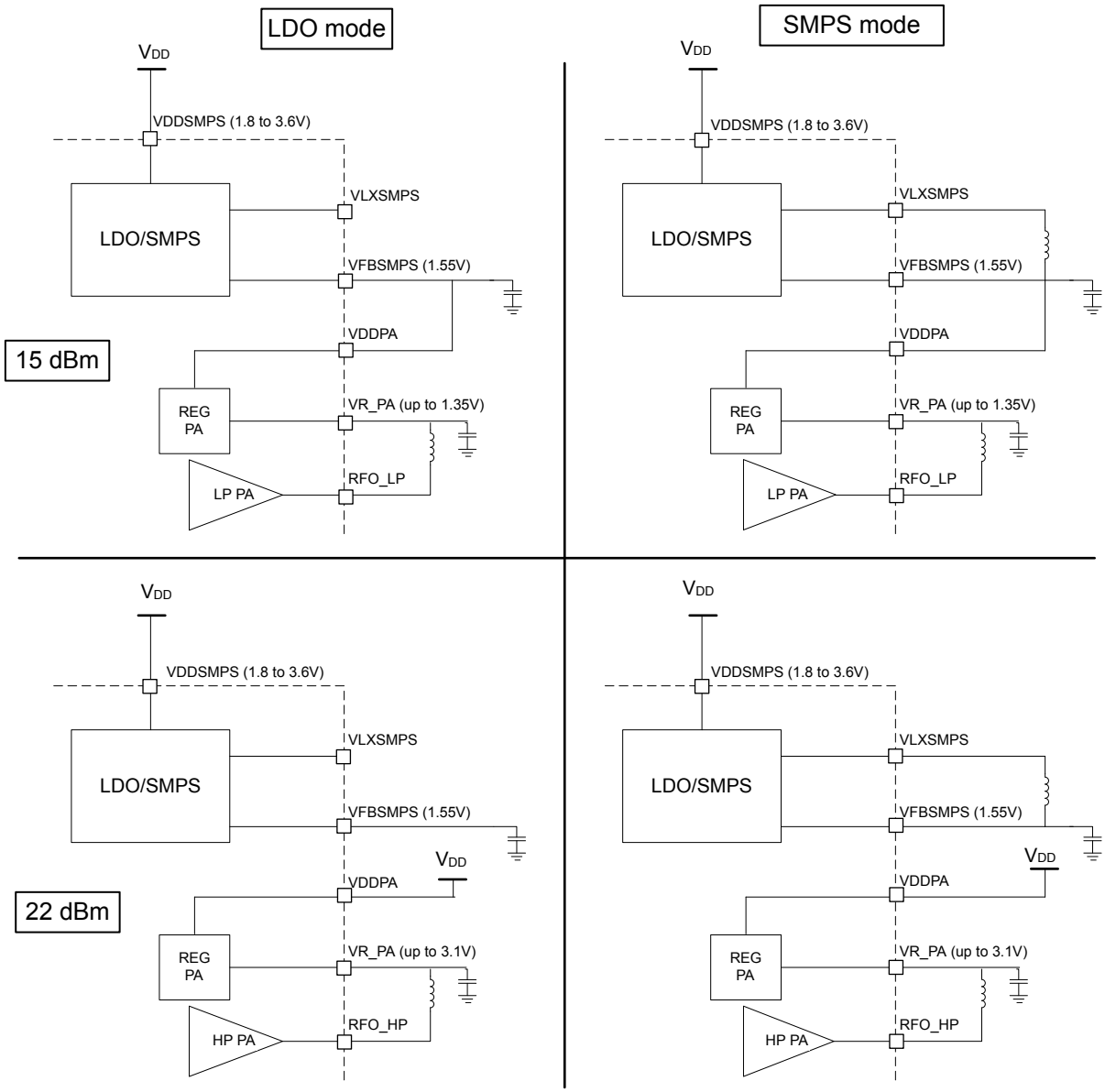
Depending on the application requirements, one of the following supply scheme can be chosen:

- use of LDO or SMPS (extra cost is a coil)
- use of RFO_LP or RFO_HP

Warning:

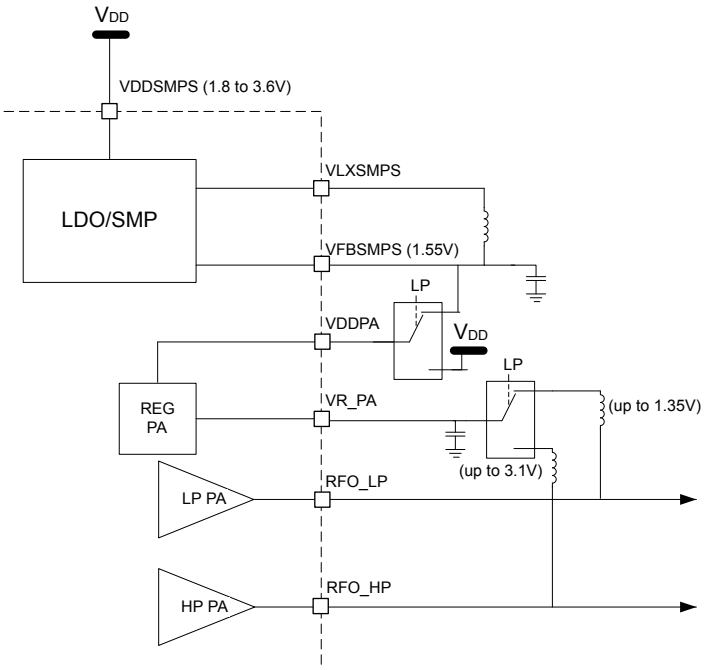
The maximum supply voltage on RFO_LP is 1.35 V maximum. This pin must not be connected to VR_PA in case RFO_HP is used. Otherwise this pin is damaged.

Figure 6. LDO/SMPS power supply schemes



When an application requires both high-power and low-power RF outputs, DC switches are required as shown below. The DC switch allows a dynamic selection of the optimum transmitter output (refer to the schematic of STM32WL Nucleo-73 board, NUCLEO-WL55JC, as an application example). DC switches can be replaced by solder bridges, if a static configuration is acceptable.

Figure 7. Power strategy supporting low and high output power



1.2.2 STM32CubeWL MCU Package

The STM32CubeWL includes a comprehensive embedded software delivered for STM32WL devices:

- CMSIS modules (core and device) corresponding to the Cortex-M4 implemented in STM32WL devices
- STM32 HAL and LL drivers: abstraction driver layer, the API ensuring maximized portability across the STM32 portfolio
- BSP drivers of each evaluation or demonstration board provided. Specific RF BSP have been implemented to support any external RF component (such as RF switch, TCXO or SMPS).
- Consistent set of middleware components such as RTOS, FatFS, LoRaWAN, KMS (key management services)
- Full set of software projects (basic examples, applications or demonstrations)

1.2.3 LoRaWAN projects

LoRaWAN projects can be found under `Projects\NUCLEO-WL55JC\Applications\LoRaWAN`.

As for I-CUBE-LRWAN, the main features of the LoRaWAN stack are listed below:

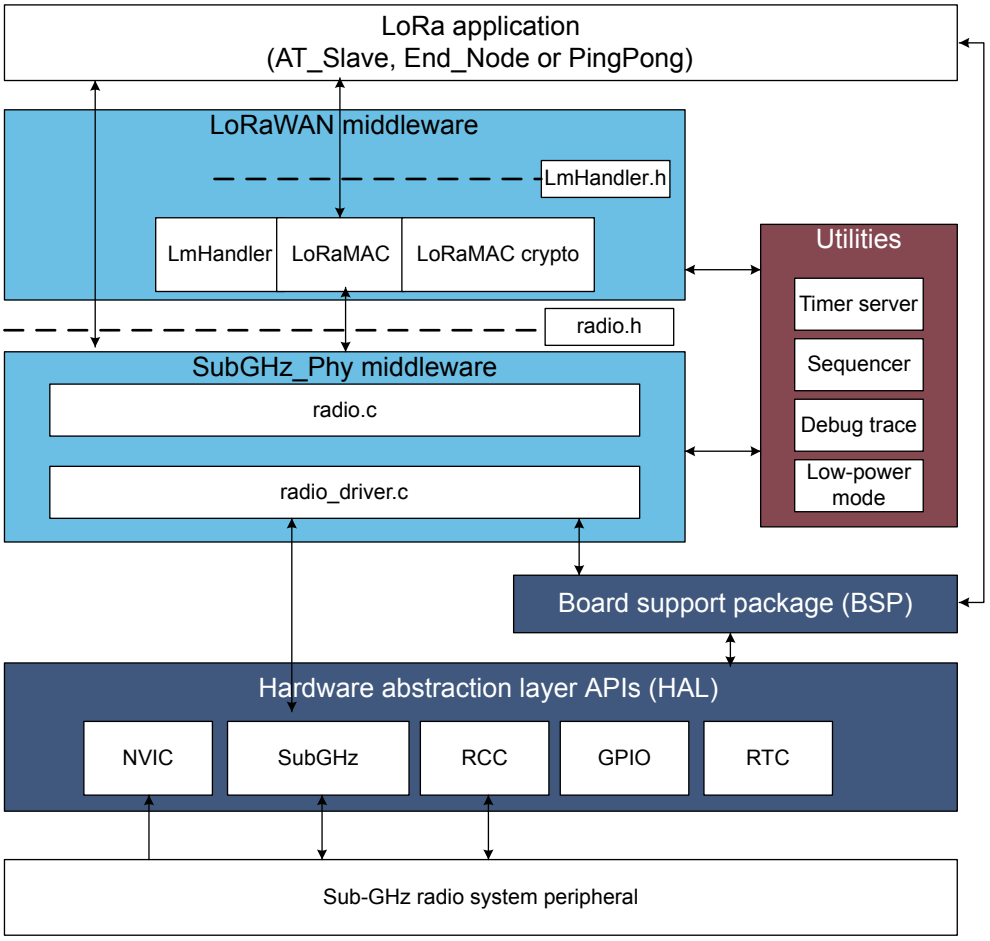
- LoRaWAN L2 V1.0.3 compatible, based on LoRaMAC-node from Semtech on GitHub.
- Supported classes:
  - Class A and Class C (Unicast and Multicast)
  - Class B
- Supported regions: `REGIONAS923`, `REGIONAU915`, `REGIONCN470`, `REGIONCN779`, `REGIONEU868`, `REGIONIN865`, `REGIONKR920`, `REGIONRU864`, `REGIONUS915`
- LoRaWAN v1.0.2 certified for `REGIONAS923`, `REGIONEU868`, `REGIONIN865`, `REGIONKR920` and `REGIONUS915`

The application is built on top of the LoRaMAC middleware. LoRaMAC APIs are the same than the one used in the I-CUBE-LRWAN.

To drive the sub-GHz radio, a new HAL (`stm32wlxx_hal_subghz.c`) has been introduced managing the initialization, the radio command and the interrupt handling.

As the configuration is hardware application dependent, the use of TCXO, RF switch types or SMPS depends on the application. The middleware needs to be aware of these specificities to ensure proper settings are applied.

Figure 8. Static LoRa architecture



The LoRaWAN stack directory structure, for I-CUBE-LRWAN and STM32CubeWL, are compared in the figure below.

Figure 9. LoRaWAN stack

2 Features of STM32WL versus STM32L0/1/4

The main features of the STM32WL devices versus STM32L0/1/4 ones are detailed in the table below.

Table 4. Main features comparison

Feature	STM32L073xx	STM32L152xx	STM32L476xx	STM32WLE5JCxx STM32WL55JCxx
Core	Cortex-M0+	Cortex-M3	Cortex-M4-F	Cortex-M4 Cortex-M0(1)
FPU	No	No	Yes	No
Max Flash memory (Kbytes)	192	512	1024	256
SRAM (Kbytes)	20	80	128	64
EEPROM (Kbytes)	6	16	No	No
OTP	No	No	Yes	Yes
Max CPU frequency (MHz)	32	32	80	48
Operating voltage	1.65 to 3.6 V	1.65 to 3.6 V	1.71 to 3.6 V	1.8 to 3.6 V
Bootloader	SPI1, USART1/ USART2, USB	SPI1, USART1/ USART2, USB	CAN1, DFU (USB device FS), I2C1/ I2C2/I2C3,SPI1/SPI2, USART1/USART2/ USART3/	SPI1/SPI2,USART1/ USART2
Advanced timers	0	0	2	1
General- purpose timers (16 and 32 bits)	4	7	7	3
Basic timers	2	2	2	0
Low-power timers	1	no	2	3
RTC	Hardware calendar	Hardware calendar	Hardware calendar	Hardware calendar and/or counter
SPI (supporting I^2S)	2(1)	3(2)	3	2(1)
QUADSPI	No	No	Yes	No
I2C	3	2	3	3
USART	4	5	5	2
LPUART	1	No	1	1
USB	USB device FS	USB device FS	OTB/FS	No
CAN	No	No	Yes	No
SWPMI	No	No	Yes	No
SAI	No	No	Yes	No
SDMMC	No	No	Yes	No
DMA (number of channels)	1 (7)	1 (12)	2 (7)	2 (7) DMA2D + DMAMUX
GPIO (max)	84	115	114	43
ADC	1	1	3	1

Feature	STM32L073xx	STM32L152xx	STM32L476xx	STM32WLE5JCxx STM32WL55JCxx
DAC	2	2	2	1
AES	No (one in STM32L08x)	No	Yes	Yes
PKA	No	No	No	Yes
RNG	No	No	Yes	Yes
UID	No	No	No	Yes
Sub-GHz radio	No	No	No	LoRa modulation, (G)FSK, (G)MSK and BPSK

1. *For STM32WL5x devices only.*

3 Peripheral migration

Only the main STM32 peripherals required to build low-power RF application are detailed below.

3.1 RCC (reset and clock controller)

Table 5. RCC features comparison

Feature	STM32L0 Series	STM32L1 Series	STM32L4 Series	STM32WL Series
HSI	HSI48, can be used after wakeup from Stop mode	8 MHz RC factory-trimmed	HI16 or HSI48 RC oscillator	HSI16, 16 MHz RC oscillator clock, can be used after wakeup from Stop mode
MSI	No	No	MSI is a low-power oscillator with programmable frequency up to 48 MHz. It can replace the PLL as system clock (faster wakeup, lower consumption). It can be used as USB device clock (no need for external high-speed crystal oscillator). Multi speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz)	RC oscillator clock from 100 kHz to 48 MHz The MSI is used as system clock source after startup from reset, configured at 4 MHz.
LSI	37 kHz RC		32 kHz RC	
HSE	1 - 32 MHz		4 to 48 MHz	HSE32, 32 MHz oscillator clock, with trimming capacitors
LSE	32.768 kHz		32.768 kHz	
PLL	Main PLL		One PLL with three outputs 2 + PLL for SAI, USB,ADC	One PLL with three outputs
System clock source	HSE, HSI, MSI or PLL			HSE32, HSI16, MSI or PLL
System clock frequency	Up to 32 MHz, MSI = 2.097 MHz after reset		Up to 80 MHz	Up to 48 MHz
APB clock frequency	Up to 32 MHz			
RTC clock Source	HSE, LSE or LSI		HSE32, LSE or LSI	
MCO clock source	HSE, HSI, HSI48, MSI, LSI, LSE, PLL, SYSCLK	HSE, HSI, MSI, LSI, LSE, PLL, SYSCLK	HSE, HSI16, MSI, LSI, LSE, PLLCLK, SYSCLK	HSE32, HSI16, MSI, LSI, LSE, PLLCLK, SYSCLK

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration:

- performance versus V_{CORE} ranges
- peripheral access configuration
- peripheral clock configuration

3.2 Power

Table 6. Power features comparison

Product	Power supply	Power supply supervisor
STM32L0 Series	• V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator, provided externally through VDD pins • V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RC and PLL (minimum voltage to be applied to VDDA pin is 1.8 V when ADC is used). VDDA and VSSA pins must be connected to VDD and VSS pins, respectively. • V_{REF+}: input reference voltage, only available as an external pin on a few packages, otherwise bonded to VDDA • V_{DD_USB}: dedicated independent USB power supply for full speed transceivers	Integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a Brownout reset (BOR) circuitry Two available versions: • BOR activated at power-on operates between 1.8 and 3.6 V. • BOR operates between 1.65 and 3.6 V.
STM32L1 Series	• V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator, provided externally through VDD pins • V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RC and PLL (minimum voltage to be applied to VDDA pin is 1.8 V when ADC is used). VDDA and VSSA pins must be connected to VDD and VSS pins, respectively. • V_{REF+}: input reference voltage, only available as an external pin on some packages, otherwise bonded to VDDA	
STM32L4 Series	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (VDDIO1), for the internal regulator and the system analog blocks such as reset, power management and internal clocks. Provided externally through VDD pins. • V_{DDA} = 1.62 (ADCs/COMPs) / 1.8 (DACs/OPAMPs) to 3.6 V: external analog power supplies for ADCs, DACs, OPAMPs, COMPs and VREFBUF. V_{DDA} voltage is independent from V_{DD}. • V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers • V_{DDIO2} = 1.08 to 3.6 V: external power supply for 14 I/Os. V_{DDIO2} voltage is independent from V_{DD}. • V_{LCD} = 2.5 to 3.6 V: the LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. • V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz.	Brownout reset (BOR) active in all modes except Shutdown (min BOR level is 1.71 V). Devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

Product	Power supply	Power supply supervisor
STM32WL Series	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, for the system analog blocks such as reset, LDO/SMPS, internal clocks and low-power regulator, provided externally through VDD pins • V_{DDA} = 1.62 (ADCs/COMPs), 1.8 (DACs/OPAMPs), 2.4 (VREFBUF) to 3.6 V: external analog power supplies for ADCs, DACs, OPAMPs, COMPs and VREFBUF. • V_{DDSMPS} = 1.7 to 3.6 V: external power supply for the SMPS step-down converter. • V_{DDRF} = 1.7 to 3.6 V: external power supply for the sub-GHz radio, provided externally through the VDDRF pin. Must be connected to the same supply as VDD pins. • V_{BAT} = 1.55 to 3.6V: power supply for RTC, TAMP, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. • $V_{DDRF1V5}$ = 1.45 to 1.62 V: external power supply for the sub-GHz radio, provided externally through the VDDRF1V5 pin • V_{REF-}, V_{REF+}: input reference voltage for the ADC. Output of the internal VREFBUF when enabled: – When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA} . – When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}.	Brownout reset (BOR) active in all modes except Shutdown (min BOR level is 1.71 V). Devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

3.3 Low-power modes and wakeup sources

There are only small changes between STM32L4 and STM32WL devices (see the table below).

For all STM32L0/1/4 devices in Stop mode, since V_{CORE} is kept on all peripherals, their registers does not have to be re-initialized when exiting Stop mode. On STM32WL devices, most peripherals are not retained by default to gain further current consumption in Stop 2 mode. These peripherals must then be re-initialized at Stop mode exit.

Table 7. Low-power modes and wakeup sources comparison

Low-power mode	STM32L0 Series	STM32L1 Series	STM32L4 Series	STM32WL Series
LPRun	No peripheral sleeping			
Sleep	Any peripheral interrupt/wakeup event			
Stop	Any EXTI line event/ interrupt (COMP, I2C, LPTIM, LPUART, PVD, RTC, USART,USB)	Any EXTI line event/ interrupt (COMP, I2C, LPUART, LPTIM,PVD, RTC, USART, USB)	Stop 0, Stop 1 and Stop 2 (BOR, COMP1/2, I2C3, IWDG, LCD, LPUART1, LPTIM1, PVD, PVM, RTC)	Stop 0, Stop 1 and Stop 2 Any EXTI line and specific peripherals events
Standby	Reset pin WKUPx pins rising edge RTC wakeup, IDWG reset	Reset pin WKUPx pins rising edge RTC wakeup, IDWG reset	Reset pin WKUPx pins rising edge RTC wakeup, IDWG reset, BOR	Reset pin WKUPx pins rising edge RTC wakeup, IDWG reset, BOR, RFIRQ wakeup, RFBUSY event, LSECSS external
Shutdown	Not supported	Not supported	Reset pin, five I/Os (WKUPx), RTC	WKUP pin edge, RTC and TAMP event, external reset in NRST pin

3.4 RTC (real-time clock)

STM32L0/1/4 and STM32WL devices implement almost the same features on the RTC (see the table below). The main difference is the introduction of a 32-bit sub-seconds counter running down to Standby mode.

Table 8. RTC features

Products	RTC features
STM32L0 Series	Coarse digital calibration (kept for compatibility only). New developments must only use smooth calibration. Two anti-tamper detection pins and 20-byte backup registers
STM32L1 Series	Coarse digital calibration (kept for compatibility only). New developments must only use smooth calibration. One tamper pin and 128-byte backup registers
STM32L4 Series	Only smooth calibration available Three tamper pins (available in VBAT) and 128-byte backup registers
STM32WL Series	Binary alarm on 32 sub-second counters Three tamper pins and 80-byte backup registers

3.5 SPI interface

The SPI/I^2S interface can be used to communicate with external devices using the SPI protocol or the I^2S audio protocol. The SPI or I^2S mode is selectable by software.

The SPI Motorola® mode is selected by default after a device reset. The SPI protocol supports half-duplex, full-duplex and simplex-synchronous serial communication with external devices.

The SPI interface is the same in STM32WL and STM32L0/1/4 devices.

3.6 USART and LPUART

USART1 and USART2

The following standard features are supported by all STM32L0/1/4 and STM32WL devices:

- asynchronous communication: IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode
- asynchronous communication Smart Card mode and SPI Master
- up to 4 Mbit/s communication

USART1/2 in STM32WL devices provide in addition, the 'wakeup MCU from Stop mode' capability, with baud-rates up to 200 kbauds.

LPUART1

Only a 32.768 kHz clock (LSE) is needed to allow LPUART1 communication up to 9600 bauds. Therefore, even in Stop mode, the LPUART1 can wait for an incoming frame while having an extremely low-energy consumption. Higher speed clock can be used to reach higher baud-rates.

3.7 General purpose I/Os (GPIOs)

The GPIOs have the same features in STM32L0/1/4 and in STM32WL devices:

Minor adaptation of the code may be required due to the following:

- mapping of particular function on different GPIOs
- alternate function selection differences

The main GPIO features are:

- GPIO mapped on AHB bus for better performance
- I/O pin multiplexer and mapping: the pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, no conflict can occur between peripherals sharing the same I/O pin.
- more possibilities and features for I/Os configuration

For more information on the GPIOs programming and usage, refer to product reference manuals and datasheets.

3.8 Flash memory and SRAM

The STM32WL devices feature up to 256 Kbytes of Flash memory and up to 64 Kbytes of SRAM1/2.
SRAM2 can be retained in Standby mode.

Note: SRAM1 is not available one STM32WLE5J8I6 devices.

3.9 Sub-GHz radio

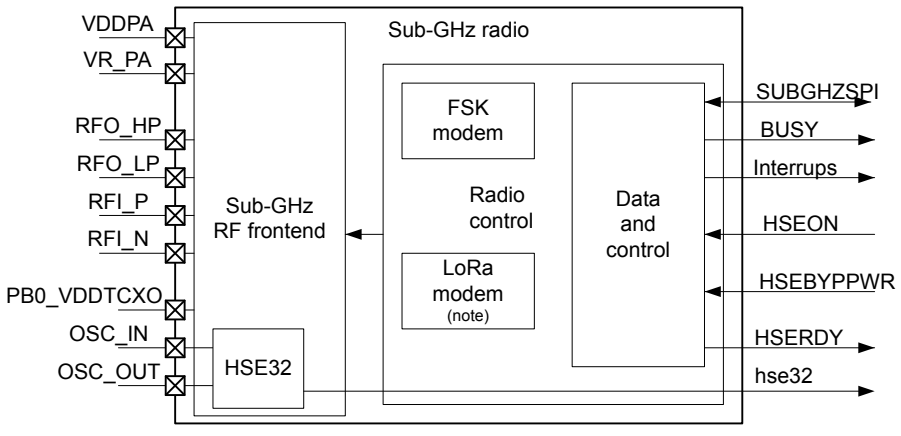
The STM32L0/1/4 devices do not embed any radio. An external radio must be attached on a board to allow RF connection.
The STM32WL devices embed within the SoC, a sub-GHz radio peripheral featuring:

- an analog front-end transceiver, capable of outputting +15 dBm maximum power on its RFO_LP pin and +22 dBm maximum power on the RFO_HP pin
- a digital modem bank providing the following modulation schemes:
  - LoRa Rx/Tx with bandwidth (BW) from 7.8 to 500 kHz, spreading factor (SF) from 5 to 12, bitrate (BR) from 0.013 to 17.4 Kbit/s
  - FSK and GFSK Rx/Tx, with BR from 0.6 to 300 Kbit/s
  - MSK and GMSK Rx/Tx, with BR from 1.2 to 300 Kbit/s, and Tx only with BR from 0.1 to 1.2 Kbit/s
  - BPSK and DBPSK Tx only, with bitrate for 100 and 600 bit/s
- a digital control comprising all data processing and sub-GHz radio configuration control
- a high-speed clock generation
- a connection to the rest of the system via an internal reserved SPI

The figure below details the sub-GHz radio interface:

- The left-hand side signals are pins connected to the package interfacing PCB.
- The right-hand side signals are internal signals connected to the rest of the SoC.

Figure 10. Sub-GHz radio block diagram



Note: LoRa modem is only available on STM32WLE5xx devices.

Revision history

Table 9. **Document revision history**

Date	Version	Changes
20-Dec-2019	1	Initial release.
13-Nov-2020	2	Updated: • Title and content to include the full STM32WL Series • Figure 9. LoRaWAN stack • Table 4. Main features comparison Added Figure 5. Sub-GHz radio peripheral in STM32WL5x devices.

Contents

List of tables

List of figures